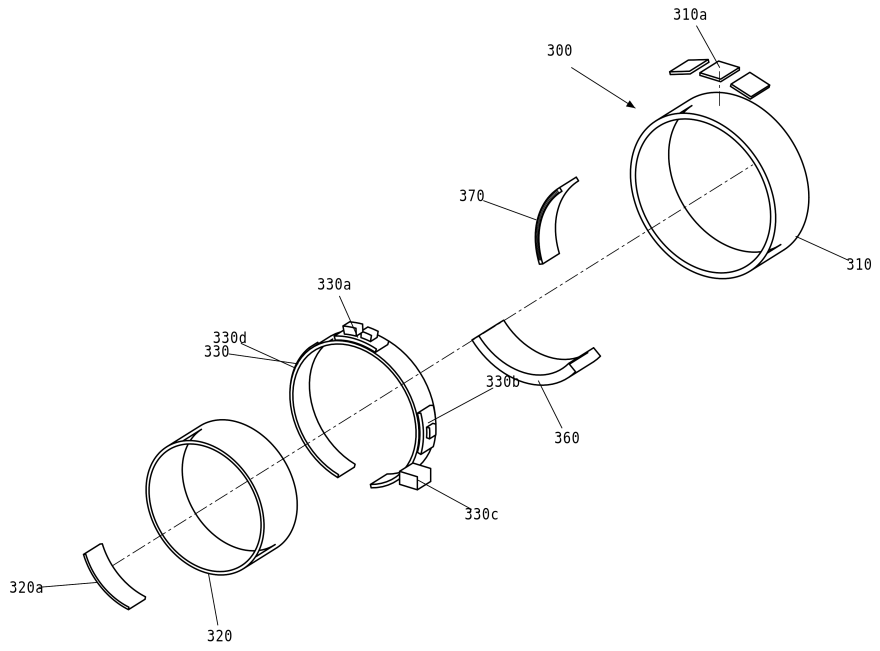
Kyra R1 EV1 - the escalation ring engine

Design documentation package



300 RING ASSEMBLY · 310 OUTER SHELL, ZIRCONIA OR Ti · 310a TOUCH STRIP, 3 PADS + GUARD · 320 INNER LINER, POTTED · 320a WEAR ELECTRODE
330 RIGID-FLEX LOOP · 330a RIGID ISLAND, CONTROLLER (nRF52833 · AT42QT1070 · KX022) · 330b RIGID ISLAND, HAPTIC (DRV2605L) · 330c LRA · 330d NFC ANTENNA
360 CELL, CURVED Li-Po 20 mAh · 370 RECEIVE COIL, 6.78 MHz · NO MICROPHONE, NO CAMERA, NO OPTICAL OR ELECTRICAL BIOSENSOR (KYR-002)

F I G . 2

Document number	KYRA-DDP
Revision	`c19ab02`
Issue date	2026-09-02
Status	DRAFT
Classification	CONFIDENTIAL
Prepared by	copperhead create pipeline, ring EV1 attempt-02
Source	`23 documents`

Document control

Revision history

Revision	Date	By	Description
c19ab02	2026-09-02	animesh-chouhan	copperhead: create pipeline stage: part-selection
370678f	2026-09-02	animesh-chouhan	copperhead: create pipeline stage: architecture
786b723	2026-09-02	animesh-chouhan	copperhead: create pipeline stage: spec-seed
c8c5b5f	2026-09-02	animesh-chouhan	stageMaxTurns: part-selection 80 (I27 workaround)
f4a625b	2026-09-02	copperhead-harness	workspace baseline: brief

Contents of this package

Part	Document	Source
I	Kyra R1 EV1 - the escalation ring engine	brief.md
II	Kyra R1 EV1 - Specification	docs/SPEC.md
III	Kyra R1 EV1 - Subsystem architecture	docs/SUBSYSTEMS.md
IV	Kyra R1 EV1 - Bill of materials	docs/BOM.md
V	DECISIONS	docs/DECISIONS.md
VI	Design changelog	docs/CHANGELOG.md
VII	Capability: Cell, Protection and Charging	openspec/specs/cell-charging/spec.md
VIII	Capability: Controller and Radio	openspec/specs/controller-radio/spec.md
IX	Capability: Haptic Escalation Channel	openspec/specs/haptic-escalation/spec.md
X	Capability: Bring-up and Instrumentation	openspec/specs/instrumentation/spec.md
XI	Capability: Motion Interlock	openspec/specs/motion-interlock/spec.md
XII	Capability: Pairing and Identity	openspec/specs/pairing-identity/spec.md
XIII	Capability: Power Budget	openspec/specs/power-budget/spec.md
XIV	Capability: Thumb Interface	openspec/specs/thumb-interface/spec.md
XV	Capability: Wireless Receive Front End	openspec/specs/wireless-receive/spec.md
XVI	Proposal: architecture-subsystem-decomposition	openspec/changes/architecture-subsystem-decomposition/proposal.md
XVII	Tasks	openspec/changes/architecture-subsystem-decomposition/tasks.md
XVIII	Proposal: part-selection-bom-ev1	openspec/changes/part-selection-bom-ev1/proposal.md
XIX	Tasks	openspec/changes/part-selection-bom-ev1/tasks.md
XX	Proposal: seed-kyra-r1-ev1-requirements	openspec/changes/seed-kyra-r1-ev1-requirements/proposal.md
XXI	Tasks	openspec/changes/seed-kyra-r1-ev1-requirements/tasks.md
XXII	Attempt 01 - FAIL (operator stop)	/home/animesh/copperhead/kyra/run-logs/2026-09-02T02-32-40/attempt-01/REPORT.md
XXIII	Attempt 02 - FAIL (operator stop at the stage-4 boundary; stages 1 to 3 committed)	/home/animesh/copperhead/kyra/run-logs/2026-09-02T02-32-40/attempt-02/REPORT.md

Contents

PART I

Kyra R1 EV1 - the escalation ring engine

Source: brief.md

Design the electronics for **Kyra R1**, the wearable confirm surface for the Kyra agent: the thing on your hand that buzzes when an open loop genuinely needs you, and that you answer with your thumb. Kyra's own words are "ambient glasses controlled by a ring: reply, dismiss or confirm with your thumb". This board is that ring's electronics.

The board specified here is **EV1**, the engineering-validation build. It carries the complete ring architecture in packages that can be ordered, assembled and probed today. The production ring is a rigid-flex assembly in wafer-level packages; EV1 is its electrical twin, and every part below names its production equivalent. EV1 exists to answer four questions before anyone spends a rigid-flex tooling cycle, and those four questions are what every requirement in this brief serves.

Why a ring, and why this ring

Kyra's software runs on Mac and iOS. The glasses are not the winnable half of the roadmap: one vendor holds most of the category and the waveguide supply, the ring-plus-glasses pair already ships from at least one competitor, and the platform vendors arrive in 2027. The hardware Kyra can own is the confirm surface.

Every smart ring shipping today is a **capture** device: it carries an optical heart-rate stack, and often a microphone. That is what makes those rings expensive in current, and it is what makes them a consent problem. Kyra R1 is a **control** device. It captures nothing. There is no microphone, no camera, no photoplethysmography, no skin-contact electrode of any kind. Its only inputs are a thumb on a touch strip and an accelerometer that decides whether the hand meant it; its only output is a vibration you can feel and nobody else can see. That is the differentiator, it is the direct hardware expression of Kyra's "your data stays with you", and it is the reason this design has a power budget the capture rings cannot match.

What EV1 must prove

1. **Gesture integrity.** Does a three-gesture thumb grammar survive a wet hand, a pocket and a handshake, on a self-capacitance controller with one guard channel?
2. **Escalation legibility.** Is a sub-100 ms LRA pulse legible on a finger, and does the supply hold up while the radio is connected?
3. **The power budget, measured.** Does the design hold 150 uA average, on an instrument, not on a spreadsheet?
4. **The charging link.** Does an induction link at ring-coil scale deliver the programmed charge current through a rectifier whose diode capacitance is not the dominant loss?

Every test point, jumper and connector on this board exists for one of those four. Nothing else is instrumented.

Scope and the parts budget

One board, one schematic sheet. Hold it to roughly **85 placed symbols** and never more than **105**, connectors, passives and test points included. Requirement text is free; only parts cost sheet area. Where a choice exists between an integrated part and a discrete block, take the integrated one unless a requirement below says otherwise. Do not add circuitry that is not listed as a board requirement; every block below is required and nothing else is.

Three assemblies are deliberately **off the board**, on connectors: the cell, the receive coil, and the linear resonant actuator. The touch electrodes are also off-board, on a flexible tail, because their geometry is the experiment.

Decisions closed

The product copy leaves these open. A schematic needs a value, so each is closed here with its reason.

1. **The controller is the nRF52833, and it runs straight off the cell.** It is the only Nordic part in the installed symbol libraries with **VDDH high-voltage mode**: 1.8 V to 5.5 V on VDDH, an internal REG0 down to VDD and REG1 to the core. A Li-Po at 4.2 V is above the 3.6 V VDD limit of the nRF52832, so choosing the 52832 would force an external regulator onto a board where every part is a millimetre of finger. The 52833 deletes that regulator. Production ring: nRF52833-CLAA WLCSP, or an nRF54L-series part once one is available in a library, on the same architecture.
2. **A dedicated touch controller, not touch on the SoC and not a second MCU.** The SoC has no charge-transfer peripheral, and a GPIO or comparator method costs a continuous stream of wake-ups. A standalone burst-mode controller scans autonomously and raises one CHANGE interrupt when something happens, so the SoC sleeps between gestures. That is the whole power budget. The published open-ring reference uses a *second microcontroller* for the same job; this design does not, because one autonomous controller with an interrupt gets the same result with one less die.
3. **Self capacitance with a guard channel, and the wet-hand result is a measurement, not an assumption.** Mutual capacitance rejects water films and body loading better, and is what the open-ring reference chose after prototyping. Self capacitance is smaller, cheaper and available now. The guard channel is therefore **mandatory, not optional**, and question 1 above is precisely the test of whether this was the right call. If it fails, the production ring moves to a mutual-capacitance controller and nothing else in the architecture changes.
4. **A confirm is gated on the accelerometer.** The documented failure mode of every gesture wearable is a false trigger when the hand is doing something else. A confirm gesture is only accepted when the accelerometer reports the hand raised and settled. This is why an accelerometer is on the board at all; it is an interlock, not a sensor feature, and no activity, sleep or step data is derived from it.
5. **Haptic energy comes from a capacitor bank, not from the cell.** A 20 mAh cell at its 3C limit delivers about 60 mA. An LRA draws well over 100 mA at start. Driving it directly browns out the radio and ages the cell. A bulk bank on the driver's own supply node, fed from the cell through a series impedance, is a hard requirement.
6. **No LED on the ring.** An indicator on your hand is a notification other people can read, which contradicts the product. The escalation channel is haptic and nothing else. EV1 carries exactly one charge-status LED, in the instrumentation block, and it is not in the ring build.
7. **No external flash.** The SoC's internal flash dual-banks a ring-sized application and holds the pending-escalation queue. The rings that carry external NOR carry it to buffer optical waveforms, which this ring does not have. Fewer parts, and the queue is small because the ring stores **opaque escalation identifiers and a haptic pattern index, never message content**. Say that in the specification; it is a product claim, not an implementation detail.
8. **No battery-sense divider.** The SoC measures its own VDDH internally through the analog-to-digital converter's internal divider input. That deletes a divider, a switch to stop it leaking, and the routing for both.
9. **Charging is inductive, and the receive front end is discrete.** The ring is sealed and hand-washed; an exposed contact is the seal that fails first. The front end is a coil, a resonant capacitor, a Schottky bridge, a clamp and a bulk capacitor. It is deliberately **not** a low-frequency wireless-power receiver integrated circuit: the ring's coil is a megahertz-class part, and a low-frequency receiver would be thrown away at the flex spin. Diode **parasitic capacitance** is the selection criterion for the bridge, ahead of forward voltage.
10. **Pairing is confirmed with the same thumb gesture the product is built on.** No PIN, no account, no cloud. Near-field out-of-band pairing where the host supports it, and a press-to-confirm on the ring itself where it does not.

Board requirements

1. Controller and radio

- **KYR-101.** Multiprotocol Bluetooth Low Energy system-on-chip, Arm Cortex-M4F, with **VDDH high-voltage mode** so the cell connects to it directly: the nRF52833 in QFN-40 (`MCU_Nordic:nRF52833_QDxx`). No external regulator on the logic rail.
- **KYR-102.** High-voltage supply network per the vendor's reference: VDDH decoupling, the REG0 output to VDD, DEC4 and the DCC inductor network for the internal DC-DC converter, and decoupling on every VDD pin. The internal DC-DC must be usable; do not populate a topology that forces LDO-only operation.
- **KYR-103.** 32 MHz crystal with its load capacitors, meeting the vendor's frequency tolerance for Bluetooth Low Energy. 32.768 kHz crystal with load capacitors for the real-time counter, because the ring keeps time between connections.
- **KYR-104.** 2.4 GHz chip antenna with a three-element pi matching network and a 50 ohm controlled-impedance path from the radio pin. Leave all three pi positions populated as placeholders so the network can be tuned on the bench; the ring will have a printed antenna and the match will be re-derived there.
- **KYR-105.** Reset provision and a pull-up on the reset pin.
- **KYR-106.** The radio shall be able to hold **two concurrent links**, to a host and to a head-worn display, without a second radio. This is a firmware and stack requirement; the board's obligation is not to preclude it.

2. Thumb interface

- **KYR-201.** Seven-channel burst-mode capacitive touch controller with an I2C interface and a CHANGE output: `Sensor_Touch:AT42QT1070-M`. It scans autonomously in low-power mode and interrupts the controller; the controller does not poll it.
- **KYR-202.** Channel allocation, fixed: **three channels** as a linear strip along the ring's outer face (tap position and swipe direction), **one channel as the guard** encircling the strip, **one channel as the wear-detect electrode** on the inner face. Two channels spare and terminated per the datasheet.
- **KYR-203.** The electrodes are **not on this board**. They leave on a six-way flat-flex connector (three strip, one guard, one wear, one ground) so electrode geometry, pitch and guard width can be changed without a board spin. Electrode geometry is the experiment; a fixed copper pattern would defeat it.
- **KYR-204.** Series resistors on every electrode line, close to the controller, for electrostatic discharge and radiated-emissions control. The value is a design decision; record it and the reason.
- **KYR-205.** Adjacent key suppression and the guard channel shall both be enabled. Record in the specification that the wet-hand result is a measurement to be taken, not a claim.
- **KYR-206.** Wear detection gates the product's behaviour: the ring **shall not** raise a haptic escalation and **shall not** accept a confirm when it reads as not worn. Hardware obligation is the electrode and the channel; the rule is firmware and belongs in the specification.

3. Motion interlock

- **KYR-301.** Three-axis accelerometer with an on-chip wake-up engine and a sample buffer, low-power current in single-digit microamps, I2C: `Sensor_Motion:KX022-1020`. Its interrupt line goes to the controller.
- **KYR-302.** Accelerometer only. No gyroscope, no magnetometer: raise-and-settle is an accelerometer question and a gyroscope costs current for nothing.
- **KYR-303.** No motion data leaves the ring. The accelerometer's output is consumed locally as the confirm interlock and is not logged, transmitted or aggregated. State this in the specification.

4. Haptic escalation channel

- **KYR-401.** Linear resonant actuator driver with automatic resonance tracking and an I2C interface: `Driver: DRV2605LDGS`. Resonance tracking is what keeps a short pulse crisp; an open-loop driver blurs it.
- **KYR-402.** The driver's enable pin is on a controller GPIO and is held low when idle, so the driver contributes nanoamps, not microamps, to the standby budget.
- **KYR-403.** A coin linear resonant actuator on a two-way connector. It is off-board: the actuator is a mechanical selection that will change, and its resonant frequency and start current are open items.
- **KYR-404. Haptic capacitor bank** on the driver's supply node, fed from the cell through a ferrite bead or series resistance so the actuator's start transient is drawn from the bank and not from the cell. Size the bank from the actuator's start current and the intended pulse length, and state the calculation in the specification. Provide the bank as at least two parallel low-equivalent-series-resistance capacitors.
- **KYR-405.** The haptic vocabulary needs at least three distinguishable patterns: something needs you, sent, dismissed. Hardware obligation is bandwidth and rise time; the patterns are firmware.

5. Cell, protection and charging

- **KYR-501.** Single curved lithium-polymer cell, 20 mAh nominal, 3.7 V, on a two-way connector so cells can be swapped during the power study. It is a bare cell with no protection module of its own.
- **KYR-502.** Discrete cell protection on the board: over-charge, over-discharge and over-current, using a protection controller and a common-source pair of low on-resistance N-channel MOSFETs in the cell's negative leg (`Battery_Management:AP9101CK` class). Non-negotiable: a bare pouch cell in a sealed product worn on a finger has no other protection.
- **KYR-503.** Linear charge management controller, programmable to the low current a 20 mAh cell needs: `Battery_Management:MCP73831-2-OT`. Program it for **15 mA** with the resistor its datasheet's programming equation gives, and state both the resistor and the equation. Fifteen milliamps is 0.75 C on this cell and fills it in about 1.6 hours, which is the charge time the category expects.
- **KYR-504.** Charge-status output to the controller, so the ring knows it is on the dock, and to the single instrumentation LED of decision 6.
- **KYR-505.** Thermal check: state the charger's worst-case dissipation at 15 mA from the clamped rectifier voltage, and confirm the package handles it.

6. Wireless receive front end

- **KYR-601.** Receive coil on a two-way connector. Coil geometry, inductance and quality factor are open items and will change during the link study.
- **KYR-602.** Series resonant capacitor sized with the coil for the link frequency, with a second footprint in parallel so the resonance can be trimmed on the bench.
- **KYR-603.** Full-wave rectifier from Schottky diodes selected for **low parasitic capacitance** at the link frequency, not for lowest forward voltage. Dual packages are preferred for area (`Diode:BAT54S` class).
- **KYR-604.** Clamp on the rectified node so an over-coupled or unloaded link cannot push the charger's input above its absolute maximum. A Zener or transient-voltage-suppressor diode plus a bulk capacitor sized to hold the charger's input through the ripple.
- **KYR-605.** Rectified-voltage sense into a controller analog input through a divider, so the link's delivered voltage can be logged during the link study. This is the one divider the board carries and it exists for question 4.
- **KYR-606.** The transmitter, the dock and its resonant drive are a **separate board and out of scope**. This board is the receiver only.

7. Pairing and identity

- **KYR-701.** Near-field communication tag antenna on the controller's dedicated NFC pins, with the two tuning capacitors the vendor's reference requires, brought out on a two-way connector so the antenna is a mechanical part. This is out-of-band pairing: tap the ring to the host and pair with no PIN and no account.
- **KYR-702.** Where a host does not support near-field pairing, pairing is confirmed by a deliberate gesture on the ring's own touch strip. No extra hardware; state the flow in the specification.
- **KYR-703.** No user-facing identifier, serial number readout or advertisement payload that carries anything about the wearer. The advertisement carries a rotating resolvable private address. Specification requirement.

8. Bring-up and instrumentation

- **KYR-801.** Serial wire debug on a 2x5 1.27 mm header, with the reset line included. EV1 only; the ring has test pads.
- **KYR-802. A current-measurement jumper in series with the cell's positive leg**, so the average current of question 3 can actually be measured with an instrument. This is the single most important part on the board for the purpose it exists for. Two-way header, shorting link fitted for normal operation.
- **KYR-803.** Test points, minimum set: cell positive, the rectified node, the driver's supply node ahead of and behind the bank, the controller's VDD, the touch CHANGE line, the accelerometer interrupt line, and ground. At least two ground test points, physically separated, so a scope probe can find a short return path.
- **KYR-804.** One charge-status LED with its resistor, per decision 6.
- **KYR-805.** I2C bus pull-ups, valued for the bus's total capacitance at the intended speed. One bus for the touch controller, the accelerometer and the haptic driver; confirm the three addresses do not collide and record them in the pinout.

9. Power budget

- **KYR-901.** The design target is **150 uA average** and the ceiling is **177 uA**, over a duty cycle of 40 escalations and 40 gesture interactions per day. Seventeen milliamp-hours usable from a 20 mAh cell over 96 hours is 177 uA; four days between charges is the bar the category has set.
- **KYR-902.** The specification shall carry an **itemised current table**, one row per device, each row citing a datasheet figure and a stated operating mode, summed, with the margin against KYR-901 shown. An unitemised total is not a budget.
- **KYR-903.** Every part's quiescent, standby and leakage current is checked against KYR-901 during part selection. A part whose standby current alone spends a tenth of the budget must be justified in its rationale or replaced.
- **KYR-904.** Haptic energy is amortised into the budget: state the per-pulse charge, the assumed pulses per day, and the resulting average.

Capture and sourcing rules

- Every part must resolve to a symbol installed on this machine. Confirm the symbol exists and confirm its pins before committing the part.
- Named parts indicate the reference implementation. Orderable equivalents are acceptable where a symbol or footprint is not available, provided the substitution is recorded with its reason.
- **The bill of materials is the EV1 build.** Its part numbers are the EV1 packages: the ones that can be ordered from a major distributor and assembled on a rigid board. Where the production ring uses a different package of the same silicon, name that production part in the rationale column, not in the part-number column. A part number that does not match its footprint is a defect.
- Parts orderable from major distributors. Mostly 0402 passives, no smaller.

Mechanical

- EV1: two-layer board, **20 mm x 20 mm**, one edge carrying the debug header and the current jumper, the opposite edge carrying the cell, coil and actuator connectors, and the flat-flex electrode connector on a third edge. Two mounting holes.
- The board is not the ring. It is sized to sit in a printed carrier for wear testing, and its connector placement exists so the coil, cell, actuator and electrode flex can be arranged as they will be in the ring.
- Production ring, for context and not for this board: rigid-flex, flex around 0.22 mm and flex-rigid around 0.48 mm, total band thickness under 3 mm, wafer-level packages throughout, US sizes 6 to 13.
- Keep the radio, the switching node of the internal DC-DC and the rectifier away from the touch electrode lines in layout intent, and note it in the documents.

Compliance

- EV1 is an engineering test unit and is not offered for sale. No certification is claimed or required for it.
- The production ring uses a bare radio silicon and a tuned antenna, so it needs full intentional-radiator testing rather than inheriting a module's certification. That is a known, budgeted cost of the ring form factor and it should be recorded in the specification, not discovered later.
- The induction link runs in an industrial, scientific and medical band; the obligation falls mainly on the transmitter, which is out of scope here.
- The ring's outer shell is the only skin-contact material. EV1 makes no biocompatibility claim.

Environment

- Operating: **0 to 45 degrees Celsius**, set by the cell's charge and discharge limits, not by the silicon. Every part must be rated for it.
- Storage: -20 to +60 degrees Celsius.
- EV1 carries no ingress rating. The production ring is sealed and potted for hand-washing.

Not yet specified - record as explicit assumptions or open items

- The actuator part, its resonant frequency and its start current. The bank in KYR-404 cannot be sized until this is known; size it from a stated assumption and flag it.
- The cell's permitted charge rate. KYR-503 assumes 0.75 C is acceptable; if the cell is a 0.5 C part the charger changes to one that regulates accurately at 10 mA.
- Coil geometry, inductance, quality factor and coupling, and therefore the resonant capacitor and the clamp voltage.
- The link frequency, subject to the coil selection above.
- Electrode geometry: strip pitch, guard width, and the dielectric thickness of the ring's outer shell.
- Whether the head-worn display link is a direct connection from the ring or is relayed by the host, and therefore how many concurrent links the stack must hold.
- Whether the production controller migrates to a newer low-power radio family.

Out of scope

- The glasses, any display, and any optical component.
- The transmitter and the charging dock. Separate board.

- The Mac and iOS software, the open-loop detection, and everything above the link.
- Any health sensor: no optical heart rate, no temperature, no skin impedance.
- Any audio path: no microphone, no speaker, no bone conduction.
- The ring's mechanical shell, its ceramic or metal band, and its sealing.

PART II

Kyra R1 EV1 - Specification

Source: docs/SPEC.md

Board: Kyra R1 EV1, escalation ring engine **Stage:** EV1 - engineering validation, not offered for sale **Source:** `brief.md` (requirement ids KYR-xxx are preserved verbatim from it) **Status:** Stage 1 - requirements seed. No schematic or board exists yet.

Every numeric budget in this document is also recorded in `.copperhead/constraints.json`. Every value the brief did not state is marked **ASSUMED** and is listed again in §12.

1. What the device is

Kyra R1 is the wearable **confirm surface** for the Kyra agent: a ring that vibrates when an open loop genuinely needs the wearer, and that the wearer answers with a thumb gesture - reply, dismiss, or confirm.

Kyra R1 is a **control** device, not a **capture** device. This is the product differentiator and it is enforced in hardware, not in firmware:

- No microphone, no camera, no photoplethysmography, no skin-contact electrode, no temperature or impedance sensor. There is no part on the bill of materials capable of capturing biometric or environmental data.
- The only inputs are a thumb on an off-board capacitive strip and a three-axis accelerometer used solely as a motion **interlock**.
- The only output is a haptic pulse. There is no indicator visible to anyone else.

EV1 is the electrical twin of the production ring, built in packages that can be ordered, assembled and probed today. The production ring is a rigid-flex assembly in wafer-level packages; each part below names its production equivalent in its rationale, never in its part-number column.

1.1 The four questions EV1 exists to answer

Every connector, jumper and test point on this board serves one of these. Nothing else is instrumented.

#	Question	Instrumented by
Q1	Does a three-gesture thumb grammar survive a wet hand, a pocket and a handshake, on a self-capacitance controller with one guard channel?	Off-board electrode flex (J4), TP `TCH_CHANGE`
Q2	Is a sub-100 ms LRA pulse legible on a finger, and does the supply hold while the radio is connected?	TPs either side of the haptic bank (`VBAT`, `VDRV`)
Q3	Does the design hold 150 μA average, measured on an instrument and not on a spreadsheet?	Current-measurement jumper J7 in the cell's positive leg
Q4	Does an induction link at ring-coil scale deliver the programmed charge current through a rectifier whose diode capacitance is not the dominant loss?	TP `VRECT`, `VRECT_SENSE` divider into the SoC ADC

2. Scope

2.1 In scope

One board, one schematic sheet, carrying: the controller and radio, the thumb interface front end, the motion interlock, the haptic escalation channel, cell protection and charging, the wireless receive front end, the NFC pairing front end, and the bring-up instrumentation.

Four assemblies are deliberately **off the board**, on connectors, because each is an open mechanical selection that must change without a board spin:

Assembly	Connector	Why off-board
Li-Po cell	J5, 2-way	Cells are swapped during the power study (KYR-501)
Receive coil	J6, 2-way	Coil geometry, L and Q are open items (KYR-601)
Linear resonant actuator	J3, 2-way	Resonant frequency and start current are open (KYR-403)
Touch electrodes	J4, 6-way FFC	Electrode geometry **is** the experiment (KYR-203)
NFC antenna	J8, 2-way	The antenna is a mechanical part (KYR-701)

2.2 Out of scope

- The glasses, any display, any optical component.
- The transmitter and the charging dock, including its resonant drive (KYR-606). This board is the **receiver only**.
- The Mac and iOS software, open-loop detection, and everything above the link.
- Any health sensor: no optical heart rate, no temperature, no skin impedance.
- Any audio path: no microphone, no speaker, no bone conduction.
- The ring's mechanical shell, band and sealing.

2.3 Parts budget

Item	Value	Source
Placed-symbol target	~85	KYR scope
Placed-symbol ceiling	**105, never exceeded**	KYR scope
Estimated count for the architecture below	**100** (worst case, summed in §3.7)	this document, §3.7
Minimum passive size	0402	sourcing rules
Sheets	1	KYR scope

The estimate sits above the ~85 target and below the 105 ceiling, but **the headroom is 5 symbols, not 13**: summing §3.7's per-block rows at the top of their "~" ranges gives 100. The earlier "92–98" was a range estimate that was never reconciled against its own table. The excess over target is instrumentation: nine test points and the current jumper, which KYR-802 and KYR-803 make mandatory. If the count approaches 105 during capture, the reduction comes out of MCU-rail decoupling multiplicity, never out of instrumentation - the board exists to be measured.

> **Rule:** do not add circuitry that is not listed as a board requirement. Every block in §3 is required and nothing else is.

3. Architecture

3.1 Block diagram (textual)

```
        J6 coil --> C_RES --> BAT54S bridge --> VRECT --+-- clamp 5.1 V + bulk
                                                       +-- divider --> ADC (VRECT_SENSE)
                                                       +-- MCP73831 --> VBAT_CELL
                                                                        |
J5 cell -- VBAT_CELL --[ J7 current jumper ]-- VBAT --+-- nRF52833 VDDH ----+
   |                                                  +-- R_HAP -- VDRV -- bank -- DRV2605L -- J3 LRA
CELL_NEG -- AP9101CK + dual NFET -- GND               |
                                                      +-- (REG0) --> VDD 3.0 V
                                                                     +-- AT42QT1070 -- R_series x6 -- J4
    electrode flex
                                                                     +-- KX022-1020
                                                                     +-- I2C pull-ups

nRF52833 -- ANT pi network -- chip antenna
         -- NFC1/NFC2 + 2 tuning caps -- J8
         -- SWD 2x5 1.27 mm (J1)
```

3.2 Confirmed symbols

Every active part below was confirmed present in the installed KiCad libraries before being named here (sourcing rule: *confirm the symbol exists before committing the part*).

Block	Part	lib_id	Confirmed	Production equivalent
Controller/ radio	nRF52833 QFN-40	`MCU_Nordic:nRF52833_ QDxx`	yes	nRF52833-CLAA WLCSP, or nRF54L-series
Touch	AT42QT1070	`Sensor_Touch:AT42QT1070-M`	yes	same silicon; mutual-cap part if Q1 fails
Motion	KX022-1020	`Sensor_Motion:KX022-1020`	yes	same silicon, WLCSP
Haptic driver	DRV2605L	`Driver:DRV2605LDGS`	yes	DRV2605LYZF WCSP
Cell protection	AP9101CK6	`Battery_Management: AP9101CK6`	yes (6 pins)	same class
Charger	MCP73831-2	`Battery_Management: MCP73831-2-OT`	yes	same silicon
Rectifier	BAT54S ×2	`Diode:BAT54S`	yes	low-Cj Schottky, same class
Antenna	2.4 GHz chip antenna	`Device:Antenna_Chip`	yes	printed antenna on the flex

Passives, connectors and test points use `Device:*`, `Connector*:*` and `Connector:TestPoint`.

3.3 Power tree

Rail	Net	Source	Nominal	Range	Feeds
Raw cell	VBAT_CELL	J5 cell +	3.7 V	3.0–4.2 V	J7, charger output, AP9101CK sense
System	VBAT	after J7	3.7 V	3.0–4.2 V	nRF52833 VDDH, R_HAP
Logic	VDD	nRF52833 **REG0**	**3.0 V** ASSUMED	1.8–3.3 V programmable	AT42QT1070, KX022-1020, I2C pull-ups, reset pull-up
Haptic	VDRV	VBAT via R_HAP + bank	3.5–4.2 V	≥2.7 V under droop	DRV2605L
Rectified	VRECT	coil/bridge, clamped	5.1 V	4.5–6.0 V window	MCP73831 VDD, sense divider
Ground	GND	cell − via protection FETs	0 V	-	all

There is no external regulator on the logic rail (KYR-101). The cell connects directly to VDDH (1.8–5.5 V) and the internal REG0 produces VDD.

VDD = 3.0 V is **ASSUMED** (the brief does not state it). Reason: it is inside the KX022-1020 maximum of 3.6 V, comfortably above the AT42QT1070 minimum of 1.8 V, and gives faster I2C edges than the 1.8 V REG0 default. **Firmware obligation:** REGOUT0 in UICR must be programmed to 3.0 V; the factory default is 1.8 V and a blank part will come up at 1.8 V.

3.4 Canonical net names

These names are binding for every later stage. Use them exactly.

VBAT_CELL, VBAT, CELL_NEG, GND, VDD, VDDH, VDRV, VRECT, VRECT_SENSE, SDA, SCL, TCH_CHANGE, ACC_INT, HAP_EN, CHG_STAT, SWDIO, SWDCLK, nRESET, ANT, NFC1, NFC2, LRA_P, LRA_N, COIL_1, COIL_2, E_STRIP1, E_STRIP2, E_STRIP3, E_GUARD, E_WEAR, XC1, XC2, XL1, XL2, DEC4, DCC, DCCH.

3.5 I2C bus (KYR-805)

One bus, three devices, no address collision:

Device	7-bit address	Set by
AT42QT1070	0x1B	fixed
KX022-1020	0x1E	ADDR strapped to GND
DRV2605L	0x5A	fixed

Strapping: KX022-1020 CS must be tied to VDD to select I2C (SPI otherwise); ADDR to GND for 0x1E. These are hardware strap pins, not GPIO.

Cross-domain check: the DRV2605L sits on VDRV (3.5–4.2 V) while the pull-ups are on VDD (3.0 V). The DRV2605L specifies an absolute I2C V_IH of 1.3 V, not a ratio of its own supply, so a 3.0 V bus drives it correctly. This is checked here because it is the kind of cross-rail mismatch that passes ERC and fails on the bench.

3.6 nRF52833 pin constraints (checked before any pin is assigned)

Pin(s)	Constraint	Consequence for this design
P0.09, P0.10	Default to **NFC** antenna pins (UICR `NFCPINS`)	Used as NFC (KYR-701) - leave at default, do not assign GPIO
P0.18	Default **nRESET** (UICR `PSELRESET`)	Used as reset (KYR-105) with a 10 kΩ pull-up
P0.00, P0.01	**XL1/XL2**, 32.768 kHz crystal only	Not available as GPIO (KYR-103)
P0.02–P0.05, P0.28–P0.31	Only these are **AIN0–AIN7**	`VRECT_SENSE` must land on one of these (AIN2/P0.04 ASSUMED)
VDDH	1.8–5.5 V	Cell connects directly; **never** connect the cell to VDD
DEC4, DCC	DC/DC network pins	REG1 buck populated (L1 between DCC and DEC4) so the internal DC-DC is usable (KYR-102); the 22 μA radio row assumes it is on
DCCH	**Absent from the installed symbol**	The REG0 (VDDH) buck inductor cannot be captured, so REG0 runs as an LDO at a cost of +3.5 μA (A24, open item O10). This absence is a tooling limit, not a design omission

3.7 Estimated symbol count by block

Block	Symbols
Controller, supply network, crystals	~28
Antenna and pi network	4
Reset + SWD header	2
Thumb interface (incl. **5** series R, FFC)	~12
Motion interlock	~5
Haptic (driver, bank, series R, connector)	~8
Cell, protection, charger, LED	~13
Current jumper	1
Wireless receive front end	~11
NFC	3
I2C pull-ups	2
Test points	9
Mounting holes	2
Total	**100** worst case (ceiling 105 → headroom **5**); **actual 90** after part selection, see below

Actual count after part selection (stage 3): 90 refdes (`docs/BOM.md` §1), so real headroom against the 105 ceiling is **15**, not 5. The controller block came in under its ~28–31 estimate because the Nordic reference decoupling needs fewer parts than allocated, and no DCCH inductor is fitted (open item O10). `J2` is deliberately unused: §2.1 names J1 and J3–J8 and the numbering is kept faithful to it rather than renumbered.

Subsystem ownership of every row above is in `docs/SUBSYSTEMS.md` §5. The five electrode series resistors were six until the architecture stage reconciled them against §3.4, which names five electrode nets; J4's sixth way is the flex ground return and deliberately carries no resistor (a resistor in a shield return defeats the shield). Recorded as open item O8.

4. Power budget (KYR-901 … KYR-904)

4.1 The target

Quantity	Value	Basis
Design target, average	**150 µA**	KYR-901
Hard ceiling, average	**177 µA**	17 mAh usable ÷ 96 h
Cell nominal	20 mAh, 3.7 V	KYR-501
Cell usable	17 mAh ASSUMED (85 % of nominal)	derived; the brief states 17 mAh usable
Endurance bar	96 h (4 days) between charges	KYR-901
Duty cycle	40 escalations + 40 gesture interactions per day	KYR-901

4.2 Itemised current table (KYR-902)

An unitemised total is not a budget. One row per device, each with its operating mode and the figure's origin. All figures are at `VDD = 3.0 V` / `VBAT = 3.7 V`, 25 °C.

#	Device / item	Operating mode	Current	Source
1	nRF52833	System ON, full RAM retention, RTC from 32.768 kHz LFXO, radio idle	3.2 µA	Nordic datasheet typ
2	nRF52833 radio	2 concurrent BLE links, 1000 ms connection interval, 0 dBm, DC/DC on	22.0 µA	Nordic power profiler, ASSUMED interval
3	nRF52833 CPU	80 wake events/day (40 escalations + 40 interactions), ~100 ms each at 3.5 mA	1.5 µA	derived, ASSUMED
4	AT42QT1070	Low-power burst mode, 128 ms scan interval, 7 keys	**40.0 µA**	datasheet burst duty × run current
5	KX022-1020	Wake-up (motion-detect) engine, low-power, 12.5 Hz ODR	8.7 µA	Kionix datasheet typ
6	DRV2605L	`EN` held low - shutdown (KYR-402)	1.0 µA	datasheet max
7	Haptic, escalations	40/day × 180 ms drive at 55 mA average supply (KYR-904)	4.6 µA	derived, §4.4
8	Haptic, acknowledgements	40/day × 30 ms drive at 55 mA average supply	0.8 µA	derived, §4.4
9	AP9101CK	Normal operating (protection active)	3.0 µA	datasheet typ
10	MCP73831-2	Off-dock, VDD unpowered - battery drain	2.0 µA	datasheet, **verify on instrument**
11	Rectifier + charger input	Off-dock reverse leakage, ~0 V reverse bias	0.5 µA	allowance
12	I2C + reset pull-ups	Bus idle high; active-low duty < 0.01 %	0.1 µA	derived
13	PCB, flux and capacitor leakage	-	2.0 µA	ASSUMED allowance
	Sub-total		**89.4 µA**	
	Design contingency, 20 %		17.9 µA	ASSUMED

#	Device / item	Operating mode	Current	Source
	Budget total		**107.3 µA**	

Margin: 42.7 µA against the 150 µA target (28 % headroom); 69.7 µA against the 177 µA ceiling (39 %). Predicted endurance at the budget total: 17 mAh ÷ 107.3 µA = **158 h ≈ 6.6 days**. At the 150 µA target: 113 h (4.7 days). At the 177 µA ceiling: exactly 96 h.

Part-selection delta (stage 3, `docs/BOM.md` §4). Two rows above could not be realised as written once real parts were chosen, and both got worse, not better:

Change	Row affected	Δ	Cause
Haptic bank becomes 4 × 220 µF MLCC, not 2 × 680 µF polymer	new row 6b	**+4.0 µA**	Polymer aluminium leaks tens–hundreds of µA; no polymer part is both 680 µF and quiet enough (BOM §4.1, A23/A27)
REG0 runs as an LDO, not a buck	rows 1–5, 12	**+3.5 µA**	The installed nRF52833 symbol exposes DEC4 and DCC but **no DCCH**, so the VDDH buck inductor is not capturable (BOM §4.2, A24, open item O10)

Revised sub-total 96.9 µA; revised budget total (×1.2) 116.3 µA. That is inside the 150 µA target (33.7 µA, 22 %) and inside the 177 µA ceiling (60.7 µA, 34 %) - **both product requirements still hold** - but it exceeds the derived `power.budget_total_uA` bookkeeping figure of 107.3 µA by 9.0 µA. There is no subsystem with slack to transfer from, so this is a genuine increase charged against target margin, not a transfer. Predicted endurance 146 h ≈ 6.1 days. **Open for the human** (see `docs/DECISIONS.md`): accept the increase, or fund it by moving the AT42QT1070 LP scan interval from 128 ms to 256 ms, which §4.3 already names as the first knob and which recovers ~20 µA.

Items deliberately at zero, and why:

- Charge-status LED: lit only while charging, which is not part of the 96 h discharge duty cycle. It is also absent from the ring build entirely (decision 6).
- `VRECT_SENSE` divider: sits on `VRECT`, which is 0 V off the dock, so it draws nothing from the cell. **This is why the divider is on the rectified node and not after the charger** - the same divider placed on `VBAT` would cost 2.5 µA continuously.
- Clamp Zener: reverse-biased at 0 V off the dock.
- No battery-sense divider exists (decision 8): the SoC measures VDDH through the SAADC's internal divider input. That deletes a divider, the switch that would stop it leaking, and the routing for both.
- Protection FET pair: enhanced on in normal operation, gate charge only at events.

4.3 KYR-903 review - parts spending more than a tenth of the budget

A tenth of the 150 µA target is 15 µA. Two rows exceed it and both are justified here:

- **AT42QT1070 at 40 µA (27 % of target).** This is the entire gesture surface and it is the reason the SoC can sleep. The alternative - the SoC scanning electrodes on GPIO or comparator - costs a continuous stream of wake-ups and more current, and a second MCU (as the published open-ring reference uses) costs a whole additional die (decision 2). The current scales directly with the LP scan interval: 128 ms is chosen for gesture responsiveness, and **the LP register is the first tuning knob if the measured total exceeds the ceiling** (256 ms roughly halves this row at the cost of latency).

- **BLE link maintenance at 22 μA (15 % of target).** Two concurrent links are a product requirement (KYR-106). The connection interval is the knob; 1000 ms is ASSUMED.

Every other part is single-digit microamps or better. No part was selected without checking its quiescent, standby and leakage figure against this table.

4.4 Haptic amortisation (KYR-904)

Assumed actuator (see §12): 10 mm coin LRA, ~175 Hz, Z $\approx$ 25 Ω, rated 2.0 V RMS. Average **supply** current during drive $\approx$ 55 mA at 3.7 V (0.16 W acoustic-mechanical drive through an H-bridge at ~85 % efficiency).

- Escalation pattern: 3 pulses $\times$ 60 ms = 180 ms of drive. Charge per escalation = 55 mA $\times$ 0.18 s = 9.9 mC = **2.75 μAh**. 40/day $\rightarrow$ 110 μAh/day $\rightarrow$ 110 $\div$ 24 = **4.6 μA average**.
- Acknowledgement pulse: 30 ms. Charge = 55 mA $\times$ 0.03 s = 1.65 mC = 0.46 μAh. 40/day $\rightarrow$ 18.3 μAh/day $\rightarrow$ **0.8 μA average**.
- **Total haptic contribution: 5.4 μA**, 3.6 % of the 150 μA target.

---

5. Sizing calculations

5.1 Charge current programming (KYR-503)

MCP73831 programming equation, from the datasheet:

```
I_REG = 1000 V / R_PROG
R_PROG = 1000 V / 0.015 A = 66.67 kohm
```

R_PROG = 66.5 kΩ, 1 %, 0402 (E96) $\rightarrow$ I_REG = 1000 / 66 500 = **15.04 mA**.

15 mA is 0.75 C on a 20 mAh cell and fills it in $\approx$ 1.6 h, the charge time the category expects. Caveat, recorded deliberately: 15 mA is the **bottom** of the MCP73831's programmable range, where current accuracy degrades ($\pm$10 % ASSUMED). That is acceptable at 0.75 C. It is also precisely why the open item "cell permitted charge rate" matters - if the cell turns out to be a 0.5 C part, 10 mA is below what this charger regulates accurately and the charger changes.

5.2 Charger thermal check (KYR-505)

Worst case is the constant-current phase at the lowest battery voltage, from the clamped rectifier voltage:

```
P_D = (V_IN(max clamped) - V_BAT(min in CC)) x I_CHG
    = (5.4 V - 2.9 V) x 15 mA
    = 37.5 mW  ~= 38 mW
```

SOT-23-5, θ_JA $\approx$ 230 °C/W (ASSUMED, no copper pour credit):

```
deltaT = 0.038 W x 230 degC/W = 8.7 degC
T_j(max) = 45 degC ambient + 8.7 degC = 53.7 degC  << 150 degC
```

The package handles it with large margin. Note that the low clamp voltage is what makes this trivial: a 6.8 V clamp would give (7.1 $-$ 2.9) $\times$ 15 mA = 63 mW.

5.3 Clamp voltage window (KYR-604)

Derived, not chosen arbitrarily:

```
lower bound = V_BAT(max) + charger dropout margin = 4.2 + 0.3 = 4.5 V
upper bound = MCP73831 absolute-max V_DD (7 V) - 1 V design margin = 6.0 V
```

Clamp = 5.1 V ±5 % Zener/TVS, 500 mW (e.g. MMSZ5231B class). At −5 % it is 4.85 V, still above the 4.5 V floor; at +5 % it is 5.36 V, well under the 6.0 V ceiling. The 500 mW rating is **ASSUMED**: the transmitter's maximum delivered power is out of scope (KYR-606), so the clamp's dissipation must be confirmed against the dock design.

5.4 Rectifier bulk capacitor (KYR-604)

```
ripple at f_link with C = 10 uF:  deltaV = I / (2.f.C) = 0.015 / (2 x 6.78e6 x 10e-6) ~= 0.11 mV
hold-up at 15 mA for 0.9 V droop: t = C.deltaV / I = 10e-6 x 0.9 / 0.015 = 0.6 ms
```

C_RECT = 10 µF / 16 V X5R 0805 + 100 nF 0402. Ripple is negligible. A link interruption longer than 0.6 ms simply pauses the charge, which is acceptable behaviour for a charger and is why no larger bulk is carried.

5.5 Resonant capacitor (KYR-602)

```
C_RES = 1 / ((2pif)^2.L)
      = 1 / ((2pi x 6.78 MHz)^2 x 1.0 uH) = 551 pF
```

C_RES = 560 pF C0G 0402, 50 V, with a second parallel 0402 position (unpopulated at build) for bench trimming. Both L = 1.0 µH and f = 6.78 MHz are **ASSUMED** - see §12. The value is a placeholder that will be re-derived once the coil exists; the second footprint is what makes that a bench change instead of a board spin.

5.6 Haptic bank and series element (KYR-404)

This is a hard requirement, not an optimisation: a 20 mAh cell at its 3 C limit delivers ~60 mA, and an LRA draws well over 100 mA at start. Driving it from the cell browns out the radio and ages the cell.

Assumptions (all ASSUMED, all in §12): LRA start/overdrive peak 150 mA for 10 ms; steady drive supply current 55 mA; firmware inhibits haptics below `VBAT` = 3.5 V; DRV2605L minimum supply 2.5 V, so `VDRV` floor = 2.7 V with margin.

```
allowed total drop        deltaV = 3.5 V - 2.7 V = 0.8 V
series R to bound the cell to its 3 C limit:
    R_HAP >= deltaV / I_cell(max) = 0.8 / 0.060 = 13.3 ohm   ->  R_HAP = 15 ohm
    cell contribution at full droop = 0.8 / 15 = 53 mA  <= 60 mA  [x]
bank must supply the start excess:
    I_bank = 150 mA - 53 mA = 97 mA for 10 ms  ->  Q = 0.97 mC
    C >= Q / deltaV = 0.97 mC / 0.8 V = 1213 uF
```

Bank = 2 × 680 µF / 6.3 V polymer aluminium, ESR ≤ 25 mΩ each (1360 µF total). Actual droop = 0.97 mC / 1360 µF = **0.71 V**, inside the 0.8 V budget. Two parallel low-ESR parts as KYR-404 requires; the footprints accept 470 µF–1000 µF so the bank can be re-sized once the actuator is measured.

Superseded at part selection (stage 3). No polymer aluminium part is both 680 µF and quiet enough for a single-digit-µA idle budget - that class specifies leakage in the tens to hundreds of microamps. **Fitted instead: C31–C34, 4 × 220 µF 6.3 V X6S 1210 MLCC**, 880 µF nominal and ≈ 308 µF effective after 65 % DC-bias

derating at 3.7 V (ASSUMED A23). The rail then supports ≈ 78 mA of start current, not the 150 mA of A5, so **firmware must cap the DRV2605L overdrive registers until O1 closes**. Bank leakage is budgeted at 1 μA/part (A27) and must be measured on J7 - open item O9. See `docs/BOM.md` §4.1. Also found there: at the 55 mA drive of A6 the drop across R_HAP is 0.83 V, putting `VDRV` 30 mV **below** the A9 floor at the A8 inhibit threshold - open item O11.

A series resistor, not a ferrite bead. A bead is ~0 Ω at DC and would not bound the cell's current at all; the DC resistance is the entire mechanism. Drop at 15 mA idle recharge = 0.23 V; drop at 53 mA = 0.8 V.

Derived firmware constraint: bank recharge time constant τ = 15 Ω × 1360 μF = 20.4 ms; 99 % recharge ≈ 5τ ≈ 102 ms. **Pulses within a pattern must be spaced ≥ 150 ms**, so a three-pulse escalation pattern occupies ≥ 450 ms. Peak recharge current = 0.8 / 15 = 53 mA, within the cell's 3 C limit ✓.

5.7 I2C pull-ups (KYR-805)

Bus capacitance C_b ≈ 50 pF ASSUMED (3 devices at ~10 pF plus ~20 pF of trace on a 20 mm board; the I2C limit is 400 pF). Fast-mode, 400 kHz, t_r(max) = 300 ns, VDD = 3.0 V.

```
R_max = t_r / (0.8473 . C_b) = 300 ns / (0.8473 x 50 pF) = 7.08 kohm
R_min = (VDD - V_OL) / I_OL = (3.0 - 0.4) / 3 mA = 867 ohm
```

R_SDA = R_SCL = 4.7 kΩ 0402. Rise time = 0.8473 × 4700 × 50 pF = **199 ns** ✓; sink current = 2.6 / 4700 = 0.55 mA, far below the 3 mA any device must sink ✓. The AT42QT1070 supports 400 kHz, which sets the bus speed.

5.8 Electrode series resistors (KYR-204)

1 kΩ, 0402, 5 %, on all five electrode lines, placed hard against the AT42QT1070. (`E_STRIP1..3`, `E_GUARD`, `E_WEAR` - the five nets named in §3.4. J4's sixth way is the flex ground return and carries **no** series resistor: resistance in a shield return defeats the shield it exists to provide. Reconciled at architecture stage; open item O8.)

Reason, recorded as KYR-204 requires: the resistors are there for ESD current limiting and radiated-emissions control on lines that leave the board on a flex tail. With a typical electrode capacitance of 5–20 pF, 1 kΩ gives an RC of ≤ 20 ns - negligible against the charge-transfer burst timing, which is on the microsecond scale, so acquisition is unaffected. 1 kΩ is the low end of the QTouch design guide's 1 kΩ–10 kΩ recommendation; the low end is chosen because the electrode leads are long (flex tail) and additional series resistance would degrade sensitivity. Acceptable tuning range 470 Ω–4.7 kΩ.

5.9 Rectified-voltage sense divider (KYR-605)

This is the **only** divider on the board, and it exists for Q4.

```
ratio = R_bot / (R_top + R_bot) = 470k / 1470k = 0.3197
V_ADC at clamp max 5.4 V = 1.73 V   (< VDD = 3.0 V  [x])
V_ADC at nominal 5.1 V   = 1.63 V
source impedance = 1 M || 470 k = 320 kohm
```

R_top = 1 MΩ, R_bot = 470 kΩ, 1 %, 0402, plus 100 nF to GND at the ADC pin. Firmware obligation: the nRF52833 SAADC needs T_ACQ = 40 μs for source impedances up to 800 kΩ; 320 kΩ requires at least 20 μs. Do not sample at the default 10 μs. Off-dock the divider draws nothing (`VRECT` = 0 V); on-dock it draws 3.5 μA from the dock, not from the cell.

5.10 Crystal load capacitors (KYR-103)

```
C_load = 2 x (C_L - C_stray),  C_stray = 2.5 pF ASSUMED
```

```
32 MHz,     C_L = 8 pF -> 2 x (8 - 2.5)  = 11 pF -> 12 pF 0402 C0G
32.768 kHz, C_L = 9 pF -> 2 x (9 - 2.5)  = 13 pF -> 12 pF 0402 C0G
```

32 MHz tolerance ±**20 ppm ASSUMED** (Nordic requires ≤ ±40 ppm total for BLE; ±20 ppm leaves room for ageing and the 0–45 °C range). 32.768 kHz ±20 ppm for the RTC, because the ring keeps time between connections.

5.11 Antenna matching network (KYR-104)

Three-element pi (shunt–series–shunt), all three positions **populated** so the network can be tuned on the bench, on a 50 Ω controlled-impedance path from the radio pin. Default population ASSUMED, chosen to be near-transparent so an un-tuned board still radiates: shunt 0.5 pF C0G 0402, series 1.0 nH high-Q 0402, shunt 0.5 pF C0G 0402. The production ring has a printed antenna and the match is re-derived there.

---

6. Behavioural rules that belong in the specification

These are firmware rules, but they are product claims and they are recorded here because the hardware exists to make them possible.

- **Wear gating (KYR-206).** When the wear-detect channel reads *not worn*, the ring **shall not** raise a haptic escalation and **shall not** accept a confirm.
- **Motion interlock (decision 4, KYR-301).** A confirm gesture is accepted only when the accelerometer reports the hand raised and settled. The accelerometer is an **interlock, not a sensor feature**.
- **No motion data leaves the ring (KYR-303).** Accelerometer output is consumed locally as the confirm interlock. It is not logged, transmitted or aggregated. No activity, sleep or step data is derived from it.
- **Queue contents (decision 7).** The pending-escalation queue in internal flash holds **opaque escalation identifiers and a haptic pattern index, never message content.** This is a product claim, not an implementation detail. It is also why no external flash is fitted: the queue is small.
- **Pairing (KYR-701, KYR-702).** Out-of-band NFC pairing where the host supports it: tap the ring to the host, no PIN, no account, no cloud. Where the host does not support it, pairing is confirmed by a deliberate gesture on the ring's own touch strip - no extra hardware.
- **Identity (KYR-703).** No user-facing identifier, serial-number readout, or advertisement payload carrying anything about the wearer. The advertisement carries a **rotating resolvable private address**.
- **Adjacent key suppression and the guard channel shall both be enabled (KYR-205).**
- **Two concurrent links (KYR-106).** Host and head-worn display, one radio. This is a firmware and stack requirement; the board's obligation is only **not to preclude it**.
- **Haptic vocabulary (KYR-405).** At least three distinguishable patterns: *something needs you*, *sent*, *dismissed*. The hardware obligation is bandwidth and rise time; the patterns are firmware.
- **Haptic inhibit below 3.5 V** (ASSUMED, derived in §5.6): protects both the droop budget and the cell.

6.1 The wet-hand result is a measurement, not a claim (KYR-205)

Self capacitance was chosen over mutual capacitance because it is smaller, cheaper and available now. Mutual capacitance rejects water films and body loading better, and is what the published open-ring reference chose after prototyping. **The guard channel is therefore mandatory, not optional.** Q1 is precisely the test of whether this was the right call. This specification makes **no claim** about wet-hand performance. If Q1 fails, the production ring moves to a mutual-capacitance controller and nothing else in the architecture changes.

7. Mechanical

Item	Value
Board	2-layer, **20 mm** × **20 mm**
Edge A	SWD header (J1) and current-measurement jumper (J7)
Edge B (opposite)	Cell (J5), coil (J6), actuator (J3) connectors
Edge C (third)	6-way FFC electrode connector (J4)
Mounting holes	2
Minimum passive	0402

The board is **not the ring**. It is sized to sit in a printed carrier for wear testing, and its connector placement exists so the coil, cell, actuator and electrode flex can be arranged as they will be in the ring.

Layout intent, to be honoured at PCB stage: keep the radio, the internal DC-DC switching node, and the rectifier **away from the touch electrode lines**. The electrode lines are high-impedance charge-transfer nodes and are the most susceptible net class on the board.

Production ring, for context and not for this board: rigid-flex, flex ≈ 0.22 mm, flex-rigid ≈ 0.48 mm, total band thickness < 3 mm, wafer-level packages throughout, US sizes 6–13.

8. Environment

Condition	Range	Set by
Operating	**0 to +45 °C**	the cell's charge and discharge limits, not the silicon
Storage	**−20 to +60 °C**	brief
Ingress	none on EV1	production ring is sealed and potted for hand-washing

Every part must be rated for the operating and storage range. This is checked at part selection: MLCC dielectric X5R or better (−55/+85 °C), polymer bank capacitors (−55/+105 °C), crystals (−40/+85 °C), all ICs industrial grade. A part rated 0/+70 °C is not acceptable because storage goes to −20 °C.

9. Compliance

- **EV1 is an engineering test unit and is not offered for sale. No certification is claimed or required for it.**
- **Recorded now so it is not discovered later:** the production ring uses bare radio silicon and a tuned antenna, so it needs **full intentional-radiator testing** (FCC Part 15C / RED EN 300 328) rather than inheriting a pre-certified module's certification. This is a known, budgeted cost of the ring form factor.

- The induction link runs in an ISM band; the regulatory obligation falls mainly on the **transmitter**, which is out of scope (KYR-606).
- The ring's outer shell is the only skin-contact material. **EV1 makes no biocompatibility claim.**

---

10. Instrumentation (KYR-801 … KYR-805)

Ref	Item	Serves
J1	SWD, 2×5, 1.27 mm, **reset line included**. EV1 only; the ring has test pads	bring-up
J7	**Current-measurement jumper, in series with the cell's positive leg**, 2-way header, shorting link fitted for normal operation	**Q3**
TP1	`VBAT_CELL` - cell positive	Q3
TP2	`VRECT` - rectified node	Q4
TP3	`VBAT` - driver supply **ahead of** the bank	Q2
TP4	`VDRV` - driver supply **behind** the bank	Q2
TP5	`VDD` - controller logic rail	Q2
TP6	`TCH_CHANGE` - touch interrupt	Q1
TP7	`ACC_INT` - accelerometer interrupt	Q1
TP8, TP9	`GND` ×2, **physically separated**, so a scope probe can find a short return path	all
D_LED + R	one charge-status LED, driven from `CHG_STAT`	KYR-804

J7 is the single most important part on the board for the purpose the board exists for: without it, Q3 is a spreadsheet answer. The AP9101CK protection network is connected on the **cell side** of J7 so the cell remains protected while the jumper is replaced by a meter.

`CHG_STAT` goes both to a controller GPIO (so the ring knows it is on the dock, KYR-504) and to the LED. **The LED is not in the ring build** (decision 6): an indicator on your hand is a notification other people can read, which contradicts the product. The escalation channel is haptic and nothing else.

---

11. Constraint and budget summary

Every row is recorded in `.copperhead/constraints.json`.

Key	Value	Source
`power.average_target_uA`	≤ 150	KYR-901
`power.average_ceiling_uA`	≤ 177	KYR-901
`power.budget_total_uA`	107.3 (incl. 20 % contingency)	§4.2
`power.cell_capacity_mAh`	20 nominal, 17 usable	KYR-501/901
`power.endurance_hours`	≥ 96	KYR-901
`power.duty_cycle`	40 escalations + 40 interactions/day	KYR-901

Key	Value	Source
`cell.max_discharge_mA`	60 (3 C)	decision 5
`charge.current_mA`	15.04 (R_PROG = 66.5 kΩ)	KYR-503
`charge.rate_C`	0.75	KYR-503
`charge.charger_dissipation_mW`	≤ 38	KYR-505
`rect.clamp_voltage_V`	$4.5 \leq V \leq 6.0$, set 5.1	KYR-604
`charger.input_abs_max_V`	7.0	MCP73831 datasheet
`mcu.vddh_range_V`	1.8 – 5.5	KYR-101
`logic.vdd_V`	3.0 (REG0) ASSUMED	§3.3
`haptic.bank_uF`	≥ 1213, fitted 1360 (2×680)	KYR-404
`haptic.series_R_ohm`	15	KYR-404
`haptic.pulse_spacing_ms`	≥ 150	§5.6
`parts.symbol_ceiling`	105 (target ~85)	scope
`parts.min_passive_size`	0402	sourcing
`board.size_mm`	20×20, 2 layers	mechanical
`env.operating_C`	0 to +45	environment
`env.storage_C`	-20 to +60	environment
`i2c.addresses`	0x1B, 0x1E, 0x5A - no collision	KYR-805
`privacy.forbidden_parts`	microphone, camera, PPG/optical HR, skin electrode, temperature, impedance	§1
`arch.forbidden_blocks`	external flash, battery-sense divider, LED in ring build, gyroscope, magnetometer, external logic regulator, second MCU, LF WPC receiver IC	decisions 2,6,7,8,9; KYR-302

12. ASSUMED values

The brief did not state these. Each is a proposed default with a reason. Each must be re-checked when the corresponding open item in §13 closes.

#	Assumption	Value	Reason	Blocks
A1	Logic rail voltage	3.0 V from REG0	Inside KX022 3.6 V max; fast I2C edges; needs UICR REGOUT0 programming	§3.3, §5.7
A2	BLE connection interval	1000 ms, 2 links, 0 dBm	Gives the 22 μA row; the knob for KYR-901	§4.2
A3	AT42QT1070 LP scan interval	128 ms	Gesture responsiveness vs the 40 μA row	§4.2, §4.3
A4	Cell usable fraction	85 % (17 mAh of 20 mAh)	Matches the brief's own 177 μA arithmetic	§4.1
A5	LRA start/overdrive current	150 mA peak for 10 ms	Typical 10 mm coin LRA; sizes the bank	§5.6
A6	LRA steady drive supply current	55 mA	2.0 V RMS into 25 Ω via H-bridge at 85 %	§4.4, §5.6

#	Assumption	Value	Reason	Blocks
A7	Escalation pattern length	3 × 60 ms; ack 30 ms	Sub-100 ms pulses per Q2	§4.4
A8	Haptic inhibit threshold	`VBAT` < 3.5 V	Protects droop budget and cell	§5.6
A9	`VDRV` floor	2.7 V (DRV2605L min 2.5 V + margin)	Droop budget	§5.6
A10	Link frequency	6.78 MHz ISM	"Megahertz-class" ring coil per decision 9	§5.4, §5.5
A11	Coil inductance	1.0 μH	Placeholder to size C_RES	§5.5
A12	Clamp power rating	500 mW	Dock delivered power is out of scope	§5.3
A13	I2C bus capacitance	50 pF	3 devices + short traces	§5.7
A14	Electrode series R	1 kΩ	ESD/EMI without harming acquisition	§5.8
A15	Crystal stray capacitance	2.5 pF	Sets load-cap value	§5.10
A16	32 MHz tolerance	±20 ppm	Margin under Nordic's ±40 ppm BLE limit	§5.10
A17	Pi network default population	0.5 pF / 1.0 nH / 0.5 pF	Near-transparent so an un-tuned board radiates	§5.11
A18	`VRECT_SENSE` ADC pin	AIN2 (P0.04)	Must be an analog-capable pin	§3.6
A19	SOT-23-5 θ_JA	230 °C/W	No copper-pour credit taken	§5.2
A20	MCP73831 accuracy at 15 mA	±10 %	Bottom of the programmable range	§5.1
A21	Design contingency	20 % on the current budget	Unmodelled leakage and firmware inefficiency	§4.2
A22	MCP73831 off-dock battery drain	2.0 μA	Datasheet figure; **verify with J7**	§4.2
A23	MLCC DC-bias derating at 3.7 V	65 % loss	220 μF 6.3 V X6S 1210 → ~77 μF effective; sizes the fitted haptic bank	§5.6, BOM §4.1
A24	REG0-as-LDO penalty	+3.5 μA	75.5 μA of VDD load at 3.0 V, LDO instead of an 85 %-efficient buck	§4.2, BOM §4.2
A25	`CHG_STAT` level shift	100 k / 100 k	STAT is push-pull to VRECT; tap = 2.55 V nominal, 2.70 V at clamp max	BOM §4.3
A26	nRF52833 DEC/decoupling values	1 μF, 100 nF, 820 pF, 47 nF	Nordic reference circuitry; confirm against the PS table before capture	BOM §1
A27	MLCC bank leakage	1 μA per part, 4 μA total	Typical for a large X6S at 3.7 V; the IR **limit** implies up to 16 μA/part - O9	§4.2, BOM §4.1

13. Open items (from the brief, recorded verbatim in intent)

These are **not** assumptions to be defended; they are unknowns that must close before the production ring. Each names what it blocks.

#	Open item	Blocks
O1	The actuator part, its resonant frequency and its start current. **The bank in KYR-404 cannot be sized until this is known**; it is sized here from A5–A7 and flagged.	§5.6, §4.4

#	Open item	Blocks
O2	The cell's permitted charge rate. KYR-503 assumes 0.75 C is acceptable; **if the cell is a 0.5 C part the charger changes** to one that regulates accurately at 10 mA.	§5.1
O3	Coil geometry, inductance, quality factor and coupling - and therefore the resonant capacitor and the clamp voltage.	§5.3, §5.5
O4	The link frequency, subject to the coil selection above.	§5.4, §5.5
O5	Electrode geometry: strip pitch, guard width, dielectric thickness of the ring's outer shell.	§5.8, Q1
O6	Whether the head-worn display link is direct from the ring or relayed by the host - and therefore how many concurrent links the stack must hold.	A2, KYR-106
O7	Whether the production controller migrates to a newer low-power radio family.	§3.2
O8	Electrode series-resistor count was stated as six in §5.8/§3.7 while §3.4 names five electrode nets. **Reconciled to five** at architecture stage (J4's sixth way is the flex ground return, deliberately unresistored). Closes when the electrode flex geometry closes with O5.	§5.8, §3.7, `docs/SUBSYSTEMS.md` §3.6
O9	Haptic-bank leakage is budgeted at 1 μA/part typical (A27) while the MLCC insulation-resistance **limit** implies up to 16 μA/part - 65 μA for the bank, which alone would breach the ceiling. **Measure on J7, per lot, on the first assembled boards.**	§4.2, §5.6
O10	The nRF52833 symbol installed on this machine exposes DEC4 and DCC but no **DCCH**, so REG0 runs as an LDO and costs 3.5 μA (A24). Revisit if a later symbol exposes the pin: one 10 μH inductor recovers it.	§4.2, §3.6
O11	At the 55 mA drive current of A6 the drop across R_HAP is 0.83 V, so at the 3.5 V inhibit threshold (A8) `VDRV` = 2.67 V, 30 mV below the A9 floor. §5.6 mixes a 53 mA droop calculation with a 55 mA drive figure. Fix is firmware: raise the inhibit threshold to 3.6 V or cap drive at 50 mA.	§5.6, §4.4

14. Requirement index

Block	Requirements	Capability spec
Controller and radio	KYR-101 … KYR-106	`openspec/specs/controller-radio/`
Thumb interface	KYR-201 … KYR-206	`openspec/specs/thumb-interface/`
Motion interlock	KYR-301 … KYR-303	`openspec/specs/motion-interlock/`
Haptic escalation	KYR-401 … KYR-405	`openspec/specs/haptic-escalation/`
Cell, protection, charging	KYR-501 … KYR-505	`openspec/specs/cell-charging/`
Wireless receive front end	KYR-601 … KYR-606	`openspec/specs/wireless-receive/`
Pairing and identity	KYR-701 … KYR-703	`openspec/specs/pairing-identity/`
Bring-up and instrumentation	KYR-801 … KYR-805	`openspec/specs/instrumentation/`

Block	Requirements	Capability spec
Power budget	KYR-901 … KYR-904	`openspec/specs/power-budget/`

PART III

Kyra R1 EV1 - Subsystem architecture

Source: docs/SUBSYSTEMS.md

Board: Kyra R1 EV1, escalation ring engine **Stage:** 2 - architecture. No schematic or board exists yet. **Parent document:** `docs/SPEC.md`. Every number here is traced back to a SPEC section or a `.copperhead/constraints.json` key. **This document introduces no new part, no new net and no new number.** It partitions what SPEC.md already states into subsystems that own boundaries, budget and interface nets.

---

0. How to read this document

SPEC.md is organised by requirement id and by calculation. That is the right shape for answering *is this value correct*, and the wrong shape for answering *whose budget is this*. Capture and layout need the second answer, so this document restates the same board as ten ownership domains.

Three rules govern every section below.

1. **Allocation is a ceiling, not a forecast.** A subsystem may spend up to its allocated current and symbol count. Spending more is not a local decision: it requires an explicit transfer from another subsystem, recorded in `docs/DECISIONS.md` with both sides named.
2. **The 20 % contingency (17.9 μA, SPEC §4.2) is board-wide and belongs to no subsystem.** It absorbs unmodelled leakage and firmware inefficiency across the whole board. A subsystem that has overspent has not "used contingency"; it has overspent.
3. **Every net that crosses a boundary appears in §14 with exactly one producer.** If a net is not in SPEC §3.4's canonical list, it does not exist. Nets are not invented at capture.

---

1. The block diagram in prose

1.1 Power flow

Energy enters the board at exactly two places and leaves it at one.

The first entry is the **dock**. A magnetic field from a transmitter that is explicitly not part of this design (KYR-606) couples into an off-board coil on **J6**. The coil and its resonant capacitor form a tank tuned to the link frequency; a two-diode Schottky bridge rectifies it into `VRECT`, which a 5.1 V clamp holds inside a window whose lower bound is the full-charge cell voltage plus charger dropout and whose upper bound is the charger's absolute maximum input minus a margin. `VRECT` feeds one load only: the charger's input.

The second entry is the **cell** on **J5**. Its positive terminal is `VBAT_CELL`; its negative terminal is `CELL_NEG`, which reaches board ground only through the protection FET pair, so the protection IC can open the return path on over-current, over-discharge or over-charge. `VBAT_CELL` is where the charger delivers its 15 mA, and it is the cell side of the measurement jumper.

Between VBAT_CELL and the rest of the board sits **J7**, a two-way header carrying a shorting link. Everything downstream of it is VBAT. This one break in the positive leg is the reason the board exists in this form: it converts the power budget from a spreadsheet claim into an instrument reading (Q3). The protection network is deliberately on the **cell** side of J7, so removing the link to insert a meter does not remove the cell's protection.

VBAT splits two ways and no more. It goes to the SoC's **VDDH** pin - the high-voltage input, 1.8–5.5 V, which is the entire reason this part was chosen over its 3.6 V-maximum sibling - and it goes through a 15 Ω series resistor to VDRV, the haptic rail. There is no external regulator anywhere on this board. The logic rail VDD is produced *inside* the SoC by REG0 and leaves through the SoC's own pins to supply the touch controller, the accelerometer and the bus pull-ups.

Energy leaves the board through the actuator on **J3**, and in trace amounts through the charge LED (which does not exist in the ring build) and the radio.

1.2 Signal flow

A thumb touches an electrode on the off-board flex. The charge-transfer measurement happens in the **touch controller**, not in the SoC - that is what buys the SoC its sleep. The controller pulls TCH_CHANGE low; the SoC wakes, reads the key state over I^2C, and asks the **accelerometer** - over the same bus - whether the hand is raised and settled. Only if both agree is a confirm accepted. This is an interlock, not a gesture sensor, and no motion sample leaves the ring.

In the other direction, an escalation arrives over BLE. The SoC raises HAP_EN, the haptic driver comes out of shutdown, and the actuator is driven from the bank on VDRV - never directly from the cell, which would brown out the radio mid-connection.

Three signal paths never touch the rest: the SWD header, the NFC antenna pair, and the 2.4 GHz path from the radio pin through a pi network to the chip antenna.

1.3 The one-line summary

> Coil → rectifier → clamp → charger → cell → **jumper** → VDDH → internal REG0 → VDD → touch + motion over one I^2C bus → SoC decides → haptic bank → actuator.

---

2. Subsystem map

Id	Subsystem	Current allocation	Symbol allocation	Answers
S1	Cell and protection	3.0 µA	6	-
S2	Charging	2.0 µA	7	Q4 (delivery)
S3	Wireless receive front end	0.5 µA	11	**Q4**
S4	Controller and radio core	8.3 µA	31	-
S5	Connectivity (BLE + NFC)	22.0 µA	7	Q2 (link held)
S6	Thumb interface	40.0 µA	12	**Q1**
S7	Motion interlock	8.7 µA	5	Q1
S8	Haptic escalation	10.4 µA	8	**Q2**
S9	Instrumentation	0.0 µA	11	**Q3** and all
S0	Board-wide	2.0 µA	2	-
	Allocated	**96.9 µA**	**100**	

Id	Subsystem	Current allocation	Symbol allocation	Answers
	Contingency, 20 % (board-wide)	19.4 μA	-	
	Budget total / ceiling	**116.3 μA** / 150 target	**105 ceiling**	

Re-issued at part selection (stage 3), not transferred. S4 rises 4.8 $\rightarrow$ 8.3 μA because the installed nRF52833 symbol has no DCCH pin and REG0 must run as an LDO; S8 rises 6.4 $\rightarrow$ 10.4 μA because the polymer haptic bank was replaced by MLCC, whose leakage is small but not zero. No subsystem had slack to donate, so §0 rule 1's transfer mechanism does not apply - this is a genuine +7.5 μA charged against the margin between the old 107.3 μA and the 150 μA target. See `docs/BOM.md` §4.4; it is an open item for the human, recorded in `docs/DECISIONS.md`.

Two subsystems - the thumb interface and connectivity - hold 69 % of the itemised budget between them. That is a deliberate architecture, not an accident, and §3.6 and §3.5 each defend their share against SPEC §4.3's tenth-of-budget review.

---

3. Subsystem sections

3.1 S1 - Cell and protection

Purpose. Hold the only stored energy on the board and make it impossible for a fault to take the cell outside its safe window.

Parts owned. J5 (2-way cell connector), U6 `Battery_Management:AP9101CK`, the dual N-FET pair in the return path, and the protection IC's sense/delay network. **Allocation:** 6 symbols, 3.0 μA (SPEC §4.2 row 9).

Nets produced. `VBAT_CELL`, `CELL_NEG`. **Nets consumed.** `GND`.

Key values and reasoning.

- **20 mAh nominal, 17 mAh usable (85 %, ASSUMED A4), 3.7 V, single curved Li-Po.** The 17 mAh figure is what makes 177 μA the hard ceiling: 17 mAh $\div$ 96 h.
- **The cell is on a connector, not soldered down.** Cells are swapped during the power study (KYR-501); a soldered cell would make Q3 a single-cell experiment.
- **Protection switches the negative leg**, so `CELL_NEG` and `GND` are distinct nets. A low-side FET pair is what lets one IC block both discharge and charge faults.
- **Discharge ceiling 60 mA (3 C).** This number does not live here - it is spent in S8, which is why S8 carries a 15 Ω resistor rather than a ferrite bead. Recorded here because S1 is the part that would be damaged if S8 got it wrong.
- **The protection network sits on the cell side of J7** (SPEC §10). Pulling the jumper for a current measurement must not leave a bare cell.

Risk. The operating range 0…+45 °C is set by *this* subsystem's charge and discharge limits, not by any silicon on the board (SPEC §8). Every other part inherits it.

3.2 S2 - Charging

Purpose. Convert whatever the dock delivers into a correctly regulated CC/CV charge, and tell the SoC that the ring is docked.

Parts owned. U5 `Battery_Management:MCP73831-2-OT`, R_PROG, input and output capacitors, the `CHG_STAT` pull-up, and the status LED with its resistor. **Allocation:** 7 symbols, 2.0 μA (SPEC §4.2 row 10 - off-dock battery drain).

Nets produced. `CHG_STAT`. **Nets consumed.** `VRECT` (from S3), `VBAT_CELL` (to S1), `GND`.

Key values and reasoning.

Value	Setting	Why
R_PROG	**66.5 kΩ 1 % 0402**	I_REG = 1000 V / R_PROG = **15.04 mA** (SPEC §5.1)
Charge rate	0.75 C, ≈ 1.6 h fill	The rate the category expects on a 20 mAh cell
Dissipation	**37.5 mW**, ΔT 8.7 °C, T_j 53.7 °C	(5.4 − 2.9) × 15 mA in SOT-23-5, θ_JA 230 °C/W ASSUMED A19
Off-dock drain	2.0 μA, **to be verified on J7**	ASSUMED A22 - a datasheet figure standing in for a measurement

Recorded caveat. 15 mA is the *bottom* of this charger's programmable range, where accuracy degrades to ±10 % (ASSUMED A20). That is acceptable at 0.75 C and is exactly why open item O2 matters: if the cell turns out to be a 0.5 C part, 10 mA is below what this device regulates accurately and **the charger changes**. The architecture tolerates that because the charger is a single SOT-23-5 with two capacitors and one resistor - a contained substitution, not a re-architecture.

`CHG_STAT` **goes two places:** a SoC GPIO, so the ring knows it is docked (KYR-504), and the LED. **Corrected at part selection:** the MCP73831's STAT pin is **push-pull, referenced to its own V_DD** - which here is `VRECT` at 5.1 V nominal and 5.4 V at the clamp maximum - not open-drain, so no pull-up is fitted and the pin may **not** be wired to a 3.0 V GPIO directly. A 100 k / 100 k divider (R5/R6) shifts it: 2.55 V at nominal `VRECT`, 2.70 V at clamp maximum, 0 V off-dock with the bottom resistor holding the GPIO low. Its 25.5 μA is drawn from the dock, never from the cell. See `docs/BOM.md` §4.3, ASSUMED A25. The LED costs nothing against the 96 h budget because it is only lit while charging, which is not part of the discharge duty cycle - and it **does not exist in the ring build** (decision 6).

3.3 S3 - Wireless receive front end

Purpose. Answer Q4: does an induction link at ring-coil scale deliver the programmed charge current through a rectifier whose diode capacitance is not the dominant loss?

Parts owned. J6 (2-way coil connector), C_RES and its unpopulated trim position, two `Diode:BAT54S` in a bridge, the 5.1 V clamp, C_RECT (10 μF + 100 nF), and the sense divider R_TOP / R_BOT with its 100 nF ADC capacitor. **Allocation:** 11 symbols, 0.5 μA (SPEC §4.2 row 11 - off-dock reverse leakage).

Nets produced. `VRECT`, `VRECT_SENSE`. **Nets consumed.** `COIL_1`, `COIL_2` (from J6), `GND`.

Key values and reasoning.

- **C_RES = 560 pF C0G 0402**, from 1 / ((2πf)^{2}L) = 551 pF at f = 6.78 MHz, L = 1.0 μH. **Both inputs are ASSUMED (A10, A11)** and both are open items (O3, O4). The mitigation is architectural, not numerical: a **second parallel 0402 position, unpopulated at build**, so re-tuning against a real coil is a bench change instead of a board spin.
- **Schottky bridge, low junction capacitance.** At megahertz-class link frequencies the diode's C_j, not its forward drop, is the loss that decides the answer to Q4. The part class is chosen for that; the specific part is confirmed to have a symbol.

- **Clamp = 5.1 V ±5 %, 500 mW.** The window is derived, not picked: floor = V_BAT(max) 4.2 V + 0.3 V charger dropout = **4.5 V**; ceiling = charger absolute-max input 7 V − 1 V margin = **6.0 V**. At −5 % the clamp is 4.85 V (above the floor); at +5 % it is 5.36 V (under the ceiling). The low clamp is also what makes S2's thermal check trivial - a 6.8 V clamp would push charger dissipation from 38 mW to 63 mW. The 500 mW rating stays ASSUMED (A12) because the dock's delivered power is out of scope.
- **C_RECT = 10 µF + 100 nF.** Ripple at the link frequency is 0.11 mV - negligible. Hold-up at 15 mA for 0.9 V is 0.6 ms. No larger bulk is carried: a link interruption longer than 0.6 ms simply pauses the charge, which is correct behaviour for a charger.
- **Sense divider 1 MΩ / 470 kΩ → 0.3197.** At the clamp maximum of 5.4 V the ADC sees 1.73 V, safely under VDD = 3.0 V.

Why the divider is here and not on VBAT. This is the **only divider on the board**. On VRECT it draws 3.5 µA *from the dock* while docked and **exactly zero from the cell** off the dock, because VRECT is 0 V. The same divider on VBAT would cost 2.5 µA continuously - 1.7 % of the whole 150 µA target - for a measurement that is only meaningful while charging.

Firmware obligation. Source impedance is 1 M ‖ 470 k = **320 kΩ**. The SoC's SAADC must use T_ACQ ≥ 20 µs, not the 10 µs default, or the reading is wrong in a way that looks like a hardware fault.

3.4 S4 - Controller and radio core

Purpose. Be the only intelligence on the board, and be asleep almost all of the time.

Parts owned. U1 MCU_Nordic:nRF52833_QDxx, the 32 MHz and 32.768 kHz crystals with four load capacitors, the DEC4/DCC/DCCH DC-DC network, all rail decoupling, the nRESET pull-up, and the two I^2C pull-ups. **Allocation:** 31 symbols, **8.3 µA** = 3.2 (System ON, full RAM retention, LFXO RTC) + 1.5 (CPU, 80 wake events/day × ~100 ms at 3.5 mA) + 0.1 (pull-ups, bus idle high) + 3.5 (REG0 running as an LDO instead of a buck - re-issued at part selection, see below and docs/BOM.md §4.2).

Nets produced. VDD (from internal REG0), SDA, SCL (bus master), HAP_EN. **Nets consumed.** VBAT → VDDH, TCH_CHANGE, ACC_INT, CHG_STAT, VRECT_SENSE, SWDIO, SWDCLK, nRESET. **Internal:** XC1, XC2, XL1, XL2, DEC4, DCC, DCCH, ANT, NFC1, NFC2.

The power tree decision, restated because it is the load-bearing one. The cell connects to **VDDH** (1.8–5.5 V) and never to VDD (3.6 V maximum). REG0 inside the SoC produces VDD = **3.0 V** (ASSUMED A1). This deletes an entire external regulator - its quiescent current, its inductor and its footprint - and it is the reason this SoC was chosen over the nRF52832.

> **Firmware obligation, and it is a trap:** REGOUT0 in UICR must be programmed to 3.0 V. A blank part comes up at **1.8 V**. Every rail-dependent number in this document assumes 3.0 V.

Strapping and pin constraints, checked before any pin is assigned (SPEC §3.6).

Pin(s)	Constraint	Architecture consequence
P0.09, P0.10	Default to NFC by UICR NFCPINS	**Used as NFC** - left at default, never assigned GPIO
P0.18	Default nRESET by UICR PSELRESET	Used as reset, 10 kΩ pull-up, wired to J1
P0.00, P0.01	XL1/XL2 only	Not available as GPIO; the 32.768 kHz crystal is not optional (RTC keeps time between connections)
P0.02–P0.05, P0.28–P0.31	The only AIN pins	VRECT_SENSE must land here - AIN2/P0.04 ASSUMED (A18)

Pin(s)	Constraint	Architecture consequence
VDDH	1.8–5.5 V	Cell direct; **never** to VDD
DEC4, DCC, DCCH	DC-DC network	REG1 buck is populated (L1 between DCC and DEC4) and the 22 μA radio row assumes it is on. **DCCH does not exist on the installed symbol**, so the REG0 (VDDH) buck cannot be captured and REG0 runs as an LDO - see below

REG0 runs as an LDO, and it costs 3.5 μA (stage 3, `docs/BOM.md` **§4.2).** The nRF52833 symbol installed on this machine exposes DEC4 (38) and DCC (39) but **no DCCH**, and a pin that does not exist cannot be wired at capture. The REG1 buck is unaffected. 75.5 μA of VDD-side load at 3.0 V costs 72.0 μA from a 3.7 V cell through an 85 %-efficient buck and 75.5 μA through an LDO - **+3.5 μA**, 2.3 % of target. The part was chosen for VDDH's 5.5 V tolerance, not for REG0's efficiency, and that reason is untouched. Open item O10.

Crystals. C_load = 2 $\times$ (C_L $-$ C_stray) with C_stray = 2.5 pF ASSUMED: 12 pF 0402 C0G for both. 32 MHz at $\pm$20 ppm (ASSUMED A16) leaves room under Nordic's $\pm$40 ppm BLE limit for ageing and the 0…+45 °C range.

I^{2}C pull-ups: 4.7 kΩ. R_max = t_r / (0.8473 $\cdot$ C_b) = 7.08 kΩ at C_b = 50 pF ASSUMED; R_min = (3.0 $-$ 0.4) / 3 mA = 867 Ω. 4.7 kΩ gives a 199 ns rise time against the 300 ns fast-mode limit and a 0.55 mA sink. They live in S4 because S4 owns `VDD` and is the bus master; they are fitted **once**, not per device.

3.5 S5 - Connectivity: BLE antenna and NFC pairing

Purpose. Get two concurrent BLE links and out-of-band pairing off the board, and own the second-largest line in the power budget.

Parts owned. ANT1 `Device:Antenna_Chip`, the three-element pi network, J8 (2-way NFC antenna connector) and two NFC tuning capacitors. **Allocation:** 7 symbols, 22.0 μA (SPEC §4.2 row 2).

Nets produced. - **Nets consumed.** `ANT`, `NFC1`, `NFC2`, `GND`.

On the 22 μA. The current is physically drawn by the SoC in S4, but it is **owned here**, because the knob that sets it is a connectivity parameter and nothing else: two concurrent links (KYR-106) at a **1000 ms connection interval, 0 dBm, DC-DC on** (ASSUMED A2). At 15 % of the 150 μA target this row passes SPEC §4.3's review on the grounds that two links are a product requirement, not an implementation convenience. If the measured total misses the ceiling, the connection interval is the second knob to turn, after S6's scan interval.

Antenna. A three-element pi (shunt–series–shunt) on a 50 Ω controlled-impedance path, with **all three positions populated** - 0.5 pF / 1.0 nH / 0.5 pF (ASSUMED A17), chosen to be near-transparent so an un-tuned board still radiates and bring-up is not blocked on a VNA. The production ring has a printed antenna and re-derives the match; that is a known, budgeted cost, along with full intentional-radiator testing (FCC 15C / RED EN 300 328) that a bare-silicon radio cannot inherit from a module.

NFC. Two tuning capacitors and a connector - the antenna itself is a mechanical part (KYR-701) and is off-board for the same reason the coil is. Pairing is a tap, with no PIN, no account and no cloud; where a host cannot do out-of-band NFC, pairing falls back to a deliberate gesture on the ring's own touch strip, which costs **no additional hardware**. The advertisement carries a rotating resolvable private address and nothing about the wearer (KYR-703).

Layout obligation carried forward. The radio path, the DC-DC switching node and the rectifier all have to stay away from S6's electrode lines. This is stated in three places on purpose.

3.6 S6 - Thumb interface

Purpose. Answer Q1 - the question the whole product rests on: does a three-gesture thumb grammar survive a wet hand, a pocket and a handshake, on a self-capacitance controller with one guard channel?

Parts owned. U2 `Sensor_Touch:AT42QT1070-M`, five 1 kΩ series resistors, J4 (6-way FFC), the `TCH_CHANGE` pull-up, and local decoupling. **Allocation:** 12 symbols, **40.0 µA** (SPEC §4.2 row 4).

Nets produced. `TCH_CHANGE`. **Nets consumed.** `VDD`, `SDA`, `SCL`, `E_STRIP1`, `E_STRIP2`, `E_STRIP3`, `E_GUARD`, `E_WEAR`, `GND`.

Key values and reasoning.

- **1 kΩ 0402 series resistor on each of the five electrode lines, hard against the controller.** They are there for ESD limiting and radiated-emissions control on lines that leave the board on a flex tail. Against 5–20 pF of electrode this is $\leq$ 20 ns of RC - negligible against charge-transfer bursts that are microseconds long. 1 kΩ is the *low* end of the 1 k–10 k design-guide range, chosen because the flex leads are long and every extra ohm costs sensitivity, which Q1 cannot afford. Tuning range 470 Ω – 4.7 kΩ.
- **Five electrodes, five resistors, six-way FFC.** The sixth way of J4 is the **ground return for the flex, and it deliberately has no series resistor** - a resistor in a shield/return path defeats the shield it exists to provide. (SPEC §5.8 and §3.7 previously said "six series R"; the canonical net list in §3.4 names five electrode nets and this document reconciles to five. See §9.)
- **Address 0x1B**, fixed. No collision with 0x1E or 0x5A.
- `TCH_CHANGE` **is open-drain** and needs the pull-up to `VDD`; it is also brought out to TP6, because Q1 is answered with a scope on that line, not with a log.
- **Adjacent key suppression and the guard channel are both mandatory** (KYR-205), not optional. Self capacitance was chosen because it is smaller, cheaper and available now; mutual capacitance rejects water films better. **This document makes no wet-hand claim.**

On the 40 µA - 27 % of the entire target, the largest single line. It is defended, not tolerated: this subsystem is the whole gesture surface, and it is what allows the SoC in S4 to sit at 3.2 µA instead of scanning electrodes itself. The alternatives are worse in exactly the way that matters - SoC-side scanning costs a continuous stream of wake-ups, and a second MCU for touch costs an entire additional die (decision 2). The current scales directly with the low-power scan interval: **128 ms is ASSUMED (A3) for gesture responsiveness, and this register is the first knob to turn if the measured board misses the 177 µA ceiling** - 256 ms roughly halves this row at the cost of latency.

Conservatism recorded. The 40 µA figure is burst duty × run current for **7 keys**, while only 5 electrodes are fitted. The budget is therefore pessimistic in the right direction.

Why the electrodes are off-board. Electrode geometry *is* the experiment (KYR-203, open item O5). A soldered-down electrode makes Q1 unanswerable after the first build.

3.7 S7 - Motion interlock

Purpose. Tell the SoC whether the hand is raised and settled. Nothing else.

Parts owned. U3 `Sensor_Motion:KX022-1020` and its decoupling, plus the strap positions. **Allocation:** 5 symbols, 8.7 µA (SPEC §4.2 row 5).

Nets produced. `ACC_INT`. **Nets consumed.** `VDD`, `SDA`, `SCL`, `GND`.

Key values and reasoning.

- **Wake-up (motion-detect) engine, low power, 12.5 Hz ODR → 8.7 µA.** The part is never streaming; it raises `ACC_INT` and goes quiet. This mode choice *is* the 8.7 µA figure.
- **Strapping is hardware, not GPIO:** `CS` tied to **VDD** to select I^2C (the part defaults to SPI otherwise), `ADDR` tied to **GND** for address **0x1E**. Both are hard ties. Getting `CS` wrong produces a device that is present, powered, and silent on the bus.
- **3.0 V `VDD` is inside this part's 3.6 V maximum** - the constraint that set A1 in the first place. A 3.3 V rail would also have worked; the cell's 4.2 V never can, which is why nothing on this rail is fed from `VBAT`.
- `ACC_INT` is brought out to TP7 alongside `TCH_CHANGE` on TP6, because Q1 is a question about *two* signals agreeing.

Product rule this subsystem exists to keep (KYR-303). Accelerometer output is consumed locally as the confirm interlock. It is **not logged, transmitted or aggregated**, and no activity, sleep or step data is derived from it. There is no gyroscope and no magnetometer (decision 9 / KYR-302): a device that could reconstruct a hand's trajectory is a capture device, and this is a control device.

3.8 S8 - Haptic escalation

Purpose. Answer Q2: is a sub-100 ms LRA pulse legible on a finger, and does the supply hold while the radio is connected?

Parts owned. U4 `Driver:DRV2605LDGS`, R_HAP, the two-part bank, the `HAP_EN` pull-down, local decoupling and J3 (2-way LRA connector). **Allocation:** 8 symbols, **10.4 µA** = 1.0 (driver in shutdown) + 4.6 (escalations) + 0.8 (acks)

- 4.0 (MLCC bank leakage, 1 µA × 4 parts - re-issued at part selection, see below and `docs/BOM.md` §4.1).

Nets produced. `VDRV`, `LRA_P`, `LRA_N`. **Nets consumed.** `VBAT`, `HAP_EN`, `SDA`, `SCL`, `GND`.

The sizing, which is a hard requirement and not an optimisation. A 20 mAh cell at its 3 C limit delivers ~60 mA; an LRA draws well over 100 mA at start. Driving the actuator from the cell browns out the radio and ages the cell.

```
allowed droop      deltaV = 3.5 V (inhibit threshold) - 2.7 V (VDRV floor) = 0.8 V
series resistor    R_HAP >= 0.8 V / 60 mA = 13.3 ohm        -> 15 ohm
cell at full droop 0.8 / 15 = 53 mA <= 60 mA [x]
bank supplies      150 mA start - 53 mA = 97 mA for 10 ms -> Q = 0.97 mC
                   C >= Q / deltaV = 1213 uF                   -> 2 x 680 uF = 1360 uF
actual droop       0.97 mC / 1360 uF = 0.71 V <= 0.8 V [x]
```

A 15 Ω resistor, not a ferrite bead. KYR-404 permits either and the distinction is the whole mechanism: a bead is ~0 Ω at DC and would not bound the cell's current at all. The DC resistance *is* the current limit. Cost: 0.23 V drop at the 15 mA idle recharge, 0.8 V at 53 mA.

Bank: superseded at part selection - 4 × 220 µF 6.3 V X6S 1210 MLCC (C31–C34), not 2 × 680 µF polymer. Polymer aluminium leaks tens to hundreds of µA and cannot live on a board with a single-digit-µA idle budget; the honest trade is capacitance for quiet. 880 µF nominal derates to ≈ 308 µF effective at 3.7 V (65 %, ASSUMED A23), which supports ≈ 78 mA of start current rather than the 150 mA of A5 - **firmware must cap the DRV2605L overdrive registers until O1 closes**. Leakage 1 µA/part budgeted (A27), to be measured on J7 (O9). Four parallel low-ESR parts still satisfy KYR-404's requirement for a multi-part low-ESR bank. The footprints accept 470 µF–1000 µF so the bank can be re-sized once the actuator is measured - open item **O1**, and the honest position is that this bank is sized from assumptions A5–A7 and not from a datasheet.

Derived firmware constraint, which is a hardware fact in disguise. τ = 15 Ω × 1360 µF = 20.4 ms; 99 % recharge ≈ 102 ms. **Pulses within a pattern must be spaced ≥ 150 ms**, so a three-pulse escalation occupies ≥ 450 ms. Peak recharge current 53 mA, inside the 3 C limit.

Amortisation (KYR-904). 40 escalations/day × 180 ms and 40 acks/day × 30 ms at 55 mA average supply give 4.6 µA and 0.8 µA - **5.4 µA total, 3.6 % of the target**. The escalation channel that justifies the whole product costs almost nothing; the surface that listens for the answer (S6) costs seven times more.

Cross-rail hazard, checked here because ERC cannot see it. The driver sits on `VDRV` (3.5–4.2 V) while the I^2C pull-ups are on `VDD` (3.0 V). The part specifies an **absolute** I^2C V_IH of 1.3 V, not a fraction of its own supply, so a 3.0 V bus drives it correctly.

`HAP_EN` **has a pull-down.** The driver must be in shutdown (1.0 µA) before firmware runs, not floating - a floating enable on a 1 µA budget line is a 3 µA bug that only appears on a cold boot.

Two connectors, one reason. J3 is 2-way and off-board because resonant frequency and start current are open (KYR-403, O1).

3.9 S9 - Instrumentation

Purpose. Make the four questions answerable with instruments. This subsystem is why the symbol count sits above the ~85 target, and it is the last thing that may be cut.

Parts owned. J1 (SWD 2×5, 1.27 mm, reset included), J7 (current-measurement jumper), TP1–TP9. **Allocation:** 11 symbols, **0.0 µA**.

Nets consumed. `SWDIO`, `SWDCLK`, `nRESET`, `VBAT_CELL`, `VBAT`, `VRECT`, `VDRV`, `VDD`, `TCH_CHANGE`, `ACC_INT`, `GND`.

Why the allocation is exactly zero, stated so it is not read as an omission. Test points are copper. The jumper is a shorting link with milliohms of resistance. The SWD header is unconnected in normal operation. The status LED is owned by S2 and is only lit on the dock. This subsystem consumes no cell energy at all, which is the only reason it can be this generous.

J7 is the single most important part on the board for the purpose the board exists for. It breaks the cell's positive leg so a meter can replace the link. Without it, Q3 is a spreadsheet answer - and SPEC §4.2 has at least one row (the charger's 2.0 µA off-dock drain, A22) that is a datasheet number standing in for a measurement.

TP8 and TP9 are both ground and are physically separated, so a scope probe anywhere on the board can find a short return path. Two ground test points is not redundancy; a long ground lead is how a 20 ms haptic droop measurement acquires 200 mV of ringing that is not there.

Reduction rule (SPEC §2.3), restated as an ownership rule: if the symbol count approaches 105, the reduction comes out of S4's decoupling multiplicity, **never** out of S9.

3.10 S0 - Board-wide

Parts owned. Two mounting holes. **Allocation:** 2 symbols, 2.0 µA - PCB, flux and capacitor leakage (ASSUMED A13-class allowance, SPEC §4.2 row 13). Plus the 20 % contingency (17.9 µA) that belongs to no subsystem.

Board: 2-layer, **20 × 20 mm**. Edge A carries J1 and J7; the opposite edge carries J5, J6 and J3; a third edge carries J4. That arrangement exists so the coil, cell, actuator and electrode flex can be positioned as they will be in the ring - the board is not the ring, but the connector geometry rehearses it.

4. Current rollup

Subsystem	SPEC §4.2 rows	µA
S1 Cell and protection	9	3.0
S2 Charging	10	2.0
S3 Wireless receive	11	0.5
S4 Controller core	1, 3, 12	8.3
S5 Connectivity	2	22.0
S6 Thumb interface	4	40.0
S7 Motion interlock	5	8.7
S8 Haptic	6, 7, 8	10.4
S9 Instrumentation	-	0.0
S0 Board-wide	13	2.0
Allocated sub-total	rows 1–13	**96.9**
Contingency 20 % (unallocated)		19.4
Budget total		**116.3**

Re-issued at part selection: +3.5 µA REG0-as-LDO in S4, +4.0 µA MLCC bank leakage in S8.

Margin: **33.7 µA against the 150 µA target** (22 %), **60.7 µA against the 177 µA ceiling** (34 %). Predicted endurance at the budget total: 17 mAh ÷ 116.3 µA = **146 h ≈ 6.1 days**.

The allocation sums to the SPEC §4.2 itemised sub-total exactly. It has to: this document partitions that number, it does not re-derive it - and when part selection moved the sub-total from 89.4 to 96.9 µA, this table moved with it rather than absorbing the difference silently.

5. Symbol rollup

Subsystem	Symbols	Corresponding SPEC §3.7 rows
S1 Cell and protection	6	share of "Cell, protection, charger, LED ~13"
S2 Charging	7	remainder of the same row
S3 Wireless receive	11	"Wireless receive front end ~11"
S4 Controller core	31	"Controller, supply, crystals ~28" + reset pull-up + I^2C pull-ups
S5 Connectivity	7	"Antenna and pi 4" + "NFC 3"
S6 Thumb interface	12	"Thumb interface ~12" (five series R after the §9 reconciliation)
S7 Motion interlock	5	"Motion interlock ~5"
S8 Haptic	8	"Haptic ~8"

Subsystem	Symbols	Corresponding SPEC §3.7 rows
S9 Instrumentation	11	"Test points 9" + "Current jumper 1" + SWD header
S0 Board-wide	2	"Mounting holes 2"
Allocated	**100**	
Actual after part selection	**90** (`docs/BOM.md` §1)	
Ceiling	**105**	
Headroom	**15** against the actual count (5 against the allocation)	

This is the finding that matters in this section. SPEC §3.7 *originally* stated a total of "~92–98" against a ceiling of 105, which reads as roughly 13 symbols of slack. Summing its own per-block rows at the top of their "~" ranges gave **101** as written, or **100** after the electrode-resistor reconciliation in §9. Real headroom against the ceiling is **five symbols, not thirteen** - SPEC §2.3 and §3.7 were corrected to 100 in the same run that produced this document. Any later stage that plans to "add a couple of parts" is planning against the wrong number.

---

6. Interface contract

Every net crossing a subsystem boundary, with exactly one producer.

Net	Producer	Consumers	Notes
`VBAT_CELL`	S1 (J5 +)	S2 (charge output), S9 (J7, TP1)	Protection is on this side of J7
`CELL_NEG`	S1 (J5 −)	S1 (protection FETs)	Reaches `GND` only through the FET pair
`VBAT`	S9 (J7 output)	S4 (VDDH), S8 (R_HAP), S9 (TP3)	The only rail the cell drives directly
`VDD`	S4 (internal REG0)	S6, S7, S4 pull-ups, S9 (TP5)	3.0 V, ASSUMED A1, needs UICR
`VDRV`	S8 (R_HAP + bank)	S8 (driver), S9 (TP4)	Never leaves S8 except to a test point
`VRECT`	S3 (bridge + clamp)	S2 (charger input), S3 (divider), S9 (TP2)	0 V off the dock
`VRECT_SENSE`	S3 (divider)	S4 (AIN2 / P0.04)	320 kΩ source → T_ACQ ≥ 20 μs
`GND`	S1 (via protection)	all	TP8, TP9 separated
`SDA`, `SCL`	S4 (master + pull-ups)	S6 (0x1B), S7 (0x1E), S8 (0x5A)	400 kHz, set by the touch controller
`TCH_CHANGE`	S6	S4, S9 (TP6)	Open-drain, pull-up in S6
`ACC_INT`	S7	S4, S9 (TP7)	Push-pull
`HAP_EN`	S4	S8	Pull-down in S8
`CHG_STAT`	S2	S4 (GPIO), S2 (LED)	Open-drain, pull-up in S2
`SWDIO`, `SWDCLK`, `nRESET`	S4	S9 (J1)	Reset line included on the header

Net	Producer	Consumers	Notes
ANT	S4	S5 (pi → antenna)	50 Ω controlled impedance
NFC1, NFC2	S4 (P0.09/P0.10)	S5 (tuning caps → J8)	Default UICR function, no GPIO
LRA_P, LRA_N	S8	J3	Off-board actuator
COIL_1, COIL_2	J6	S3 (tank + bridge)	Off-board coil
E_STRIP1..3, E_GUARD, E_WEAR	J4	S6 (series R → controller)	Highest-impedance nets on the board
XC1, XC2, XL1, XL2, DEC4, DCC, DCCH	S4	S4	Internal, listed so nobody reassigns them

No net appears here that is absent from SPEC §3.4. No subsystem produces a net that another subsystem also produces.

---

7. Cross-domain hazards

Four mismatches that pass ERC and fail on the bench. Each is checked at architecture stage because each is cheapest to fix now.

1. **3.0 V bus into a driver on a 3.5–4.2 V rail (S4 → S8).** The DRV2605L's I^2C V_IH is an absolute 1.3 V, not a ratio of its supply, so a 3.0 V bus drives it correctly. Had it been ratiometric (0.7 × VDRV = 2.94 V) the bus would have been marginal at every corner.
2. **Cell to VDDH, never to VDD (S1 → S4).** A 4.2 V cell on a 3.6 V-maximum pin destroys the part. This is why the power tree has exactly two rails downstream of the cell and why the logic rail is produced inside the SoC.
3. **High-impedance electrode lines against the radio, the DC-DC node and the rectifier (S6 vs S4, S5, S3).** The electrode nets are the most susceptible net class on the board and the other three are the three most aggressive sources. This is a layout constraint stated at architecture time because by layout it is a placement fact, not a preference.
4. **320 kΩ ADC source impedance (S3 → S4).** Default 10 μs acquisition under-samples; the symptom is a plausible-looking wrong voltage, which is the worst kind.

---

8. Deliberate absences

A missing part looks like an oversight unless the absence is recorded. Each of these is an architectural choice with a reason.

Absent	Subsystem it would sit in	Why it is absent
External logic regulator	S4	REG0 inside the SoC does it; the cell goes to VDDH (KYR-101)

Absent	Subsystem it would sit in	Why it is absent
Battery-sense divider on `VBAT`	S1/S4	Decision 8 - the SAADC measures VDDH internally; deletes a divider, its disconnect switch and 2.5 μA
External flash	S4	Decision 7 - the queue holds opaque escalation ids and a pattern index, not content; internal flash is enough
Second MCU for touch	S6	Decision 2 - a whole additional die to do what the touch controller already does
LED in the ring build	S2	Decision 6 - an indicator on your hand is a notification other people can read
Gyroscope, magnetometer	S7	Decision 9 / KYR-302 - an interlock does not need them, and they make the ring a trajectory sensor
LF wireless-power receiver IC	S3	Decision 9 - megahertz-class link at ring-coil scale
Transmitter / dock circuitry	-	KYR-606 - this board is the receiver only
Series resistor on J4's ground return	S6	It would defeat the shield it exists to provide (§3.6)
Microphone, camera, PPG, skin electrode, temperature, impedance sensor, speaker	-	**§1 of SPEC: Kyra R1 is a control device, not a capture device.** No part on the BOM is capable of biometric or environmental capture. This is enforced in hardware, not firmware.

9. Open items by subsystem

Item	Subsystem	Blocks
O1 actuator, resonant frequency, start current	S8	Bank sizing (currently from A5–A7)
O2 cell permitted charge rate	S2	R_PROG, possibly the charger part
O3 coil geometry, L, Q, coupling	S3	C_RES, clamp voltage
O4 link frequency	S3	C_RES, C_RECT
O5 electrode geometry	S6	Series R value, Q1
O6 direct vs relayed display link	S5	Connection interval, and therefore the 22 μA row
O7 controller family migration	S4	Production part only, not EV1
O8 electrode series-resistor count: SPEC §5.8/§3.7 said six, §3.4 names five nets	S6	Reconciled to **five** here and in SPEC; J4's sixth way is the ground return
O9 (new) MLCC haptic-bank leakage: 1 μA/part budgeted, IR limit implies up to 16 μA/part	S8	The whole current budget - measure on J7 per lot
O10 (new) installed nRF52833 symbol has no DCCH pin; REG0 runs as an LDO	S4	3.5 μA; recover with one inductor if a later symbol exposes DCCH
O11 (new) at 55 mA drive (A6) the R_HAP drop puts `VDRV` 30 mV under the A9 floor at the A8 threshold	S8	Firmware: inhibit at 3.6 V or cap drive at 50 mA

10. Traceability

This document	SPEC.md
§1 block diagram in prose	§3.1
§3.1–§3.10 subsystem sections	§3.2, §3.3, §5.1–§5.11, §6
§4 current rollup	§4.1–§4.4
§5 symbol rollup	§2.3, §3.7
§6 interface contract	§3.4, §3.5, §3.6
§7 cross-domain hazards	§3.5, §3.6, §5.9, §7
§8 deliberate absences	§1, §11
§9 open items	§12, §13

PART IV

Kyra R1 EV1 - Bill of materials

Source: docs/BOM.md

Board: Kyra R1 EV1, escalation ring engine **Stage:** 3 - part selection. No schematic or board exists yet. **Parent documents:** `docs/SPEC.md`, `docs/SUBSYSTEMS.md`. Budgets live in `.copperhead/constraints.json`.

Every active part below was confirmed present in the KiCad symbol libraries installed on **this machine** with `search_symbols`, and its pin list read back with `symbol_pins`, before being written into a row. The lib_id and confirmed pin count for every refdes is in §3.

Every MPN in this document is `UNVERIFIED`. Each is a datasheet-verifiable proposal: the rationale states the parameter that must be checked, so the check is a lookup and not a re-selection.

Three SPEC values could not be realised as written. They are resolved here as recorded deviations, not as blockers - §4 states each one, its numeric cost, and the open item it leaves for the human.

1. Bill of materials

One row per refdes. No grouped rows. The Value column holds the component value only. `[Sn]` at the head of each rationale names the owning subsystem from `docs/SUBSYSTEMS.md` §2.

Refdes	Value	Footprint	MPN	Rationale
J5	Conn_01x02	Connector_JST:JST_SH_ SM02B-SRSS-TB_1x02-1MP_ P1.00mm	UNVERIFIED: JST SM02B-SRSS-TB(LF)(SN)	[S1] Li-Po cell, on a connector because cells are swapped during the power study (KYR-501); verify 1 A contact rating and −25/+85 °C in the JST SH datasheet.
U6	AP9101CK6	Package_TO_SOT_SMD:SOT-23-6	UNVERIFIED: AP9101CK6-AWDE-7	[S1] Single-cell protection, low-side FET drive. Verify overcharge 4.28 V, overdischarge 2.4 V and operating current 3.0 μA typ / 6.0 μA max against SPEC §4.2 row 9 (3.0 μA allocated).
Q1	Dual N-MOS	Package_TO_SOT_SMD:SOT-363_SC-70-6	UNVERIFIED: DMN62D0LDW-7	[S1] Protection FET pair in the CELL_NEG return, back-to-back so one IC blocks both charge and discharge faults. Verify V_DS $\geq$ 20 V, V_GS(th) < 1.5 V at 4.2 V drive, and gate leakage < 100 nA.

Refdes	Value	Footprint	MPN	Rationale
R1	330R	Resistor_SMD:R_0402_1005Metric	UNVERIFIED: Yageo RC0402FR-07330RL	[S1] AP9101 VDD sense series resistor; the standard application value that limits current into the IC during a cell hot-plug.
R2	2k	Resistor_SMD:R_0402_1005Metric	UNVERIFIED: Yageo RC0402FR-072KL	[S1] AP9101 VM pin resistor; sets charger-detection current and limits VM current during a short. Verify against the AP9101 application circuit.
C1	100nF	Capacitor_SMD:C_0402_1005Metric	UNVERIFIED: Murata GRM155R71C104KA88D	[S1] AP9101 VDD–VSS decoupling, X7R 16 V; part of the RC that gives the protection IC a stable rail during a fault event.
U5	MCP73831-2-OT	Package_TO_SOT_SMD:SOT-23-5	UNVERIFIED: Microchip MCP73831T-2ACI/OT	[S2] 4.2 V CC/CV charger, symbol confirmed at 5 pins. Verify the `-2` suffix is the 4.2 V regulation option and that battery drain with V_DD unpowered is $\leq 2.0\ \mu$A (SPEC §4.2 row 10, A22 - to be measured on J7).
R3	66.5k	Resistor_SMD:R_0402_1005Metric	UNVERIFIED: Yageo RC0402FR-0766K5L	[S2] I_REG = 1000 V / R_PROG = 15.04 mA = 0.75 C on a 20 mAh cell (SPEC §5.1). 1 %, E96. 15 mA is the bottom of the programmable range, $\pm$10 % ASSUMED (A20).
C2	4.7uF	Capacitor_SMD:C_0805_2012Metric	UNVERIFIED: Murata GRM21BR61C475KA88L	[S2] Charger V_DD input capacitor on VRECT. 16 V X5R chosen so DC-bias derating at the 5.4 V clamp maximum is small; verify effective C $\geq 3\ \mu$F at 5.4 V.
C3	4.7uF	Capacitor_SMD:C_0603_1608Metric	UNVERIFIED: Murata GRM188R61A475KE15D	[S2] Charger V_BAT output capacitor; the datasheet requires $\geq 4.7\ \mu$F for loop stability. 10 V X5R against a 4.2 V rail.
D1	Green	LED_SMD:LED_0603_1608Metric	UNVERIFIED: Würth 150060GS75000	[S2] Charge-status indicator, anode to VRECT and cathode through R4 to STAT (open-drain-style sink when charging). Lit only on the dock, so it costs nothing against the 96 h discharge budget. **Not fitted in the ring build** (decision 6).
R4	2.2k	Resistor_SMD:R_0402_1005Metric	UNVERIFIED: Yageo RC0402FR-072K2L	[S2] LED series resistor: (5.1 − 2.0) / 2.2 k = 1.4 mA, within the MCP73831 STAT 25 mA sink rating and bright enough on a bench LED.

Refdes	Value	Footprint	MPN	Rationale
R5	100k	Resistor_SMD:R_0402_1005Metric	UNVERIFIED: Yageo RC0402FR-07100KL	[S2] Top leg of the CHG_STAT level shift. **Deviation 3** (§4.3): STAT is push-pull referenced to V_DD = VRECT, so it swings to 5.1 V nominal / 5.4 V clamped and cannot drive a 3.0 V GPIO directly.
R6	100k	Resistor_SMD:R_0402_1005Metric	UNVERIFIED: Yageo RC0402FR-07100KL	[S2] Bottom leg of the same divider: tap = 2.55 V at nominal VRECT, 2.70 V at the 5.4 V clamp maximum, inside the GPIO's VDD+0.3 V limit. It also defines the GPIO as low when the charger is unpowered off-dock. Divider current 25.5 μA is drawn **from the dock**, never from the cell.
J6	Conn_01x02	Connector_JST:JST_SH_SM02B-SRSS-TB_1x02-1MP_P1.00mm	UNVERIFIED: JST SM02B-SRSS-TB(LF)(SN)	[S3] Receive-coil connector. Off-board because coil geometry, L and Q are open items O3/O4 (KYR-601).
C4	560pF	Capacitor_SMD:C_0402_1005Metric	UNVERIFIED: Murata GRM1555C1H561JA01D	[S3] Resonant capacitor: $1/((2\pi f)^2 L)$ = 551 pF at f = 6.78 MHz, L = 1.0 μH (both ASSUMED, A10/A11). C0G 50 V because the tank swings well above VRECT and a Class-2 dielectric would detune it.
C5	DNP	Capacitor_SMD:C_0402_1005Metric	- (position not fitted at build)	[S3] Second parallel C0G position for bench trimming against a real coil. Deliberately unpopulated: it turns closing O3/O4 into a bench change instead of a board spin.
D2	BAT54S	Package_TO_SOT_SMD:SOT-23	UNVERIFIED: Nexperia BAT54S,215	[S3] Half the rectifier bridge, series pair in one SOT-23. Verify junction capacitance $\leq$ 10 pF at 1 V - at megahertz-class link frequencies C_j, not V_F, is the loss that decides Q4.
D3	BAT54S	Package_TO_SOT_SMD:SOT-23	UNVERIFIED: Nexperia BAT54S,215	[S3] The other half of the bridge, same part for matched C_j. Reverse leakage 2 μA max at 25 V; off-dock the reverse bias is ~0 V, so the contribution to SPEC §4.2 row 11 (0.5 μA) is an allowance, not a datasheet worst case.

Refdes	Value	Footprint	MPN	Rationale
D4	5.1V	Diode_SMD:D_SOD-123	UNVERIFIED: onsemi MMSZ5231BT1G	[S3] VRECT clamp. Window is derived: floor 4.2 V cell + 0.3 V charger dropout = 4.5 V; ceiling 7 V charger absolute max − 1 V margin = 6.0 V. 5.1 V ±5 % sits at 4.85/5.36 V, inside both. 500 mW rating is ASSUMED (A12) - dock power is out of scope. Draws nothing from the cell because VRECT = 0 V off-dock.
C6	10uF	Capacitor_SMD:C_0805_ 2012Metric	UNVERIFIED: Murata G RM21BR61C106KE15L	[S3] Rectifier bulk. Ripple at the link frequency 0.11 mV; hold-up at 15 mA for 0.9 V is 0.6 ms. 16 V X5R for DC-bias headroom at 5.4 V.
C7	100nF	Capacitor_SMD:C_0402_ 1005Metric	UNVERIFIED: Murata G RM155R71C104KA88D	[S3] High-frequency companion to C6 at the bridge output, where the switching edges are.
R7	1M	Resistor_SMD:R_0402_ 1005Metric	UNVERIFIED: Yageo RC0402FR-071ML	[S3] Top of the VRECT sense divider, 1 %. This is the **only** divider on the board and it is on VRECT, not VBAT, so it draws 3.5 μA from the dock and exactly zero from the cell.
R8	470k	Resistor_SMD:R_0402_ 1005Metric	UNVERIFIED: Yageo RC0402FR-07470KL	[S3] Bottom of the divider: ratio 0.3197, so 5.4 V clamp maximum reads 1.73 V at the ADC, under VDD = 3.0 V. Source impedance 320 kΩ → SAADC T_ACQ $\geq$ 20 μs, not the 10 μs default.
C8	100nF	Capacitor_SMD:C_0402_ 1005Metric	UNVERIFIED: Murata G RM155R71C104KA88D	[S3] Anti-alias / charge reservoir at the AIN2 pin; with 320 kΩ source it also supplies the SAADC sampling capacitor so the acquisition does not droop the divider.
U1	nRF52833	Package_DFN_QFN:QFN-40-1EP_5x5mm_P0.4mm_ EP3.6x3.6mm	UNVERIFIED: Nordic nRF52833-QIAA-R	[S4] Controller and radio. Chosen for VDDH 1.8–5.5 V so the cell connects directly and no external regulator exists (KYR-101). Symbol confirmed at 41 pins. Verify the QIAA package is the 5×5 mm QFN-40 and that P0.09/P0.10 default to NFC.
Y1	32MHz	Crystal:Crystal_SMD_2016-4Pin_2.0x1.6mm	UNVERIFIED: Abracon ABM8-32.000MHZ-B2-T	[S4] HFXO for the radio. Verify C_L = 8 pF and total tolerance $\leq$ ±20 ppm over −40/+85 °C, which leaves margin under Nordic's ±40 ppm BLE requirement (A16).

Refdes	Value	Footprint	MPN	Rationale
Y2	32.768kHz	Crystal:Crystal_SMD_3215-2Pin_3.2x1.5mm	UNVERIFIED: Abracon ABS07-32.768KHZ-9-T	[S4] LFXO. Not optional: the RTC keeps time between connections and SPEC §4.2 row 1 (3.2 μA) is the LFXO figure, not the RC-oscillator figure. Verify C_L = 9 pF, $\pm$20 ppm, -40/+85 °C.
C9	12pF	Capacitor_SMD:C_0402_1005Metric	UNVERIFIED: Murata GRM1555C1H120JA01D	[S4] Y1 load capacitor on XC1: $2 \times (8 - 2.5)$ = 11 pF $\rightarrow$ 12 pF C0G. C_stray 2.5 pF ASSUMED (A15).
C10	12pF	Capacitor_SMD:C_0402_1005Metric	UNVERIFIED: Murata GRM1555C1H120JA01D	[S4] Y1 load capacitor on XC2, matched to C9. C0G because a Class-2 dielectric would shift the load capacitance with temperature and blow the ppm budget.
C11	12pF	Capacitor_SMD:C_0402_1005Metric	UNVERIFIED: Murata GRM1555C1H120JA01D	[S4] Y2 load capacitor on XL1: $2 \times (9 - 2.5)$ = 13 pF $\rightarrow$ 12 pF C0G, the nearest stock value.
C12	12pF	Capacitor_SMD:C_0402_1005Metric	UNVERIFIED: Murata GRM1555C1H120JA01D	[S4] Y2 load capacitor on XL2, matched to C11.
L1	10uH	Inductor_SMD:L_0805_2012Metric	UNVERIFIED: Murata LQM2HPN100MJ0L	[S4] REG1 buck inductor between DCC and DEC4, which is what makes the 22 μA radio row achievable (KYR-102). Verify I_sat $\geq$ 100 mA and DCR $\leq 1\ \Omega$. **The REG0 (VDDH) buck inductor does not exist** - see Deviation 2, §4.2.
C13	1uF	Capacitor_SMD:C_0402_1005Metric	UNVERIFIED: Murata GRM155R60J105KE19D	[S4] DEC4 capacitor, the REG1 buck output reservoir. Value from the Nordic reference circuit (A26) - confirm against the nRF52833 PS reference-circuitry table before capture.
C14	100nF	Capacitor_SMD:C_0402_1005Metric	UNVERIFIED: Murata GRM155R71C104KA88D	[S4] DEC1 decoupling, Nordic reference value (A26).
C15	100nF	Capacitor_SMD:C_0402_1005Metric	UNVERIFIED: Murata GRM155R71C104KA88D	[S4] DEC3 decoupling, Nordic reference value (A26).
C16	820pF	Capacitor_SMD:C_0402_1005Metric	UNVERIFIED: Murata GRM1555C1H821JA01D	[S4] DEC5 decoupling, Nordic reference value (A26). C0G.
C17	47nF	Capacitor_SMD:C_0402_1005Metric	UNVERIFIED: Murata GRM155R71C473KA01D	[S4] DEC6 decoupling, Nordic reference value (A26).
C18	100nF	Capacitor_SMD:C_0402_1005Metric	UNVERIFIED: Murata GRM155R71C104KA88D	[S4] VDD decoupling at pin 8, placed hard against the pin.
C19	100nF	Capacitor_SMD:C_0402_1005Metric	UNVERIFIED: Murata GRM155R71C104KA88D	[S4] VDD decoupling at pin 18.

Refdes	Value	Footprint	MPN	Rationale
C20	100nF	Capacitor_SMD:C_0402_1005Metric	UNVERIFIED: Murata GRM155R71C104KA88D	[S4] VDD decoupling serving pins 30 and 40. If the symbol count ever approaches the 105 ceiling, this multiplicity is the designated donor (SPEC §2.3) - instrumentation is never cut.
C21	4.7uF	Capacitor_SMD:C_0603_1608Metric	UNVERIFIED: Murata GRM188R61A475KE15D	[S4] VDD bulk. REG0 runs as an LDO (Deviation 2) so this reservoir carries the radio's burst current instead of a buck inductor.
C22	100nF	Capacitor_SMD:C_0402_1005Metric	UNVERIFIED: Murata GRM155R71C104KA88D	[S4] VDDH decoupling. VDDH is the cell rail - nothing here may be rated under 6.3 V.
C23	4.7uF	Capacitor_SMD:C_0603_1608Metric	UNVERIFIED: Murata GRM188R61A475KE15D	[S4] VDDH bulk, 10 V X5R against a 4.2 V rail so DC-bias derating stays modest.
R9	10k	Resistor_SMD:R_0402_1005Metric	UNVERIFIED: Yageo RC0402FR-0710KL	[S4] nRESET pull-up on P0.18 (KYR-105). Costs 0.3 μA only while the line is pulled low, which is never in normal operation.
R10	4.7k	Resistor_SMD:R_0402_1005Metric	UNVERIFIED: Yageo RC0402FR-074K7L	[S4] SDA pull-up. R_max = 300 ns / (0.8473 $\times$ 50 pF) = 7.08 kΩ, R_min = 2.6 V / 3 mA = 867 Ω; 4.7 k gives a 199 ns rise and 0.55 mA sink. Fitted once for the whole bus, not per device.
R11	4.7k	Resistor_SMD:R_0402_1005Metric	UNVERIFIED: Yageo RC0402FR-074K7L	[S4] SCL pull-up, matched to R10.
ANT1	2.4GHz	RF_Antenna:Johanson_2450AT18A100	UNVERIFIED: Johanson 2450AT18A100E	[S5] Chip antenna, symbol `Device:Antenna_Chip` confirmed at 2 pins. Verify the keep-out area fits the 20 $\times$ 20 mm outline; the production ring replaces this with a printed antenna.
C24	0.5pF	Capacitor_SMD:C_0402_1005Metric	UNVERIFIED: Murata GRM1555C1HR50BA01D	[S5] First shunt of the pi network. All three positions populated so the match can be tuned on the bench; 0.5 pF is chosen to be near-transparent so an un-tuned board still radiates (A17).
L2	1.0nH	Inductor_SMD:L_0402_1005Metric	UNVERIFIED: Murata LQP15MN1N0B02D	[S5] Series element of the pi network. Verify Q $\geq$ 20 at 2.4 GHz - a low-Q part here is an insertion loss the link budget cannot see coming.
C25	0.5pF	Capacitor_SMD:C_0402_1005Metric	UNVERIFIED: Murata GRM1555C1HR50BA01D	[S5] Second shunt of the pi network, matched to C24.

Refdes	Value	Footprint	MPN	Rationale
J8	Conn_01x02	Connector_JST:JST_SH_ SM02B-SRSS-TB_1x02-1MP_ P1.00mm	UNVERIFIED: JST SM02B-SRSS-TB(LF)(SN)	[S5] NFC antenna connector. The antenna is a mechanical part (KYR-701) so it is off-board for the same reason the coil is.
C26	300pF	Capacitor_SMD:C_0402_ 1005Metric	UNVERIFIED: Murata GRM1555C1H301JA01D	[S5] NFC1 tuning capacitor. Value must be re-derived once the antenna inductance is known; C0G so the tune does not drift with temperature.
C27	300pF	Capacitor_SMD:C_0402_ 1005Metric	UNVERIFIED: Murata GRM1555C1H301JA01D	[S5] NFC2 tuning capacitor, matched to C26 - the NFC front end is differential and an asymmetric tune costs read range.
U2	AT42QT1070	Package_DFN_QFN:QFN-20-1EP_4x4mm_P0.5mm_ EP2.5x2.5mm	UNVERIFIED: Microchip AT42QT1070-MMH	[S6] Self-capacitance touch controller, symbol `Sensor_Touch:AT42QT1070-M` confirmed at 21 pins. MODE tied to VSS selects I^2C; address 0x1B, no collision with 0x1E or 0x5A. Verify the 40 μA LP-burst figure at a 128 ms interval (A3) - this is the largest single line in the budget and the first knob to turn if the board misses the ceiling.
R12	1k	Resistor_SMD:R_0402_ 1005Metric	UNVERIFIED: Yageo RC0402FR-071KL	[S6] E_STRIP1 series resistor, hard against U2. ESD/EMI limiting on a line that leaves the board on a flex tail; RC $\leq$ 20 ns against 5–20 pF, negligible against microsecond charge-transfer bursts.
R13	1k	Resistor_SMD:R_0402_ 1005Metric	UNVERIFIED: Yageo RC0402FR-071KL	[S6] E_STRIP2 series resistor, same reasoning as R12.
R14	1k	Resistor_SMD:R_0402_ 1005Metric	UNVERIFIED: Yageo RC0402FR-071KL	[S6] E_STRIP3 series resistor, same reasoning as R12.
R15	1k	Resistor_SMD:R_0402_ 1005Metric	UNVERIFIED: Yageo RC0402FR-071KL	[S6] E_GUARD series resistor. The guard channel is mandatory, not optional (KYR-205).
R16	1k	Resistor_SMD:R_0402_ 1005Metric	UNVERIFIED: Yageo RC0402FR-071KL	[S6] E_WEAR series resistor. Wear detection gates escalation (KYR-206). 1 kΩ is the low end of the 1 k–10 k guide range because the flex leads are long and every extra ohm costs sensitivity Q1 cannot afford.

Refdes	Value	Footprint	MPN	Rationale
J4	Conn_01x06	Connector_FFC-FPC:Hirose_FH12-6S-0.5SH_1x06-1MP_P0.50mm_Horizontal	UNVERIFIED: Hirose FH12-6S-0.5SH(55)	[S6] Electrode flex connector. Five electrode ways plus a sixth that is the flex ground/shield return - **the sixth way deliberately has no series resistor**, because resistance in a shield return defeats the shield (open item O8).
R17	10k	Resistor_SMD:R_0402_1005Metric	UNVERIFIED: Yageo RC0402FR-0710KL	[S6] TCH_CHANGE pull-up to VDD. The CHANGE pin is confirmed open-collector in the symbol, so without this the line floats and the SoC never wakes.
R18	10k	Resistor_SMD:R_0402_1005Metric	UNVERIFIED: Yageo RC0402FR-0710KL	[S6] U2 ~RESET pull-up to VDD. Active-low reset with no internal pull-up; leaving it floating gives an intermittently dead touch controller.
C28	100nF	Capacitor_SMD:C_0402_1005Metric	UNVERIFIED: Murata GRM155R71C104KA88D	[S6] U2 VDD decoupling. Charge-transfer acquisition is sensitive to rail noise, so this sits at the pin.
U3	KX022-1020	Package_LGA:LGA-12_2x2mm_P0.5mm	UNVERIFIED: Kionix KX022-1020	[S7] Three-axis accelerometer used **only** as a motion interlock. Symbol confirmed at 11 pins. ~CS tied to IO_VDD selects I^2C (SPI otherwise); SDO/ADDR tied to GND gives 0x1E. Verify the 8.7 μA wake-up-engine figure at 12.5 Hz ODR. VDD 3.6 V max is the constraint that set VDD = 3.0 V.
C29	100nF	Capacitor_SMD:C_0402_1005Metric	UNVERIFIED: Murata GRM155R71C104KA88D	[S7] U3 VDD decoupling at the pin.
C30	100nF	Capacitor_SMD:C_0402_1005Metric	UNVERIFIED: Murata GRM155R71C104KA88D	[S7] U3 IO_VDD decoupling; the part has a separate I/O supply pin and the datasheet requires both decoupled.
U4	DRV2605L	Package_SO:VSSOP-10_3x3mm_P0.5mm	UNVERIFIED: TI DRV2605LDGSR	[S8] LRA driver with closed-loop auto-resonance, symbol confirmed at 10 pins, address 0x5A. Cross-rail check: its I^2C V_IH is an absolute 1.3 V, not a ratio of VDRV, so the 3.0 V bus drives it correctly. Verify shutdown current $\leq$ 1.0 μA with EN low.

Refdes	Value	Footprint	MPN	Rationale
R19	15R	Resistor_SMD:R_0805_2012Metric	UNVERIFIED: Yageo RC0805FR-0715RL	[S8] Series element between VBAT and VDRV. **A resistor, not a ferrite bead** - a bead is ~0 Ω at DC and would not bound the cell at all; the DC resistance is the entire mechanism. 0.8 V / 15 Ω = 53 mA, inside the 60 mA (3 C) cell limit. Dissipation 42 mW at 53 mA, inside an 0805's 125 mW.
R20	100k	Resistor_SMD:R_0402_1005Metric	UNVERIFIED: Yageo RC0402FR-07100KL	[S8] HAP_EN pull-down. The driver must be in shutdown before firmware runs; a floating enable on a 1 μA budget line is a several-μA bug that only shows on a cold boot.
C31	220uF	Capacitor_SMD:C_1210_3225Metric	UNVERIFIED: Murata GRM32EC80J227ME05L	[S8] Haptic bank, 1 of 4. **Deviation 1** (§4.1): the 2 × 680 μF polymer bank in SPEC §5.6 cannot be bought at single-digit μA leakage. X6S 6.3 V 1210, ~65 % DC-bias derating at 3.7 V → ~77 μF effective; four parts give ~308 μF effective against 880 μF nominal. Verify the DC-bias curve at 3.7 V.
C32	220uF	Capacitor_SMD:C_1210_3225Metric	UNVERIFIED: Murata GRM32EC80J227ME05L	[S8] Haptic bank, 2 of 4. Own refdes so the bank can be depopulated one part at a time during the O1 bench study.
C33	220uF	Capacitor_SMD:C_1210_3225Metric	UNVERIFIED: Murata GRM32EC80J227ME05L	[S8] Haptic bank, 3 of 4. X6S is −55/+105 °C, comfortably outside the −20/+60 °C storage range.
C34	220uF	Capacitor_SMD:C_1210_3225Metric	UNVERIFIED: Murata GRM32EC80J227ME05L	[S8] Haptic bank, 4 of 4. ~308 μF effective supports a ~78 mA peak for 10 ms within the 0.8 V droop budget, not the 150 mA of ASSUMED A5 - firmware must cap the DRV2605L overdrive register until O1 closes.
C35	100nF	Capacitor_SMD:C_0402_1005Metric	UNVERIFIED: Murata GRM155R71C104KA88D	[S8] U4 VDD decoupling at the pin, for the H-bridge switching edges the bank is too slow to serve.
C36	1uF	Capacitor_SMD:C_0402_1005Metric	UNVERIFIED: Murata GRM155R60J105KE19D	[S8] DRV2605L REG pin capacitor; the datasheet requires it for the internal regulator and the part will not start without it.

Refdes	Value	Footprint	MPN	Rationale
J3	Conn_01x02	Connector_JST:JST_SH_ SM02B-SRSS-TB_1x02-1MP_ P1.00mm	UNVERIFIED: JST SM02B-SRSS-TB(LF)(SN)	[S8] LRA connector. Off-board because resonant frequency and start current are open (KYR-403, O1) - the actuator is the variable the bank is sized against.
J1	Conn_02x05	Connector_PinHeader_1.27mm: PinHeader_2x05_P1.27mm_ Vertical	UNVERIFIED: Samtec FTSH-105-01-L-DV-K	[S9] SWD header, 2×5 at 1.27 mm, **reset line included** (KYR-801). EV1 only; the ring has test pads.
J7	Conn_01x02	Connector_PinHeader_1.27mm: PinHeader_1x02_P1.27mm_ Vertical	UNVERIFIED: Harwin M50-3500242	[S9] Current-measurement jumper in the cell's positive leg, shorting link fitted normally. **The single most important part on the board for the purpose the board exists for**: without it Q3 is a spreadsheet answer, and SPEC §4.2 has at least one row (A22) that is a datasheet number standing in for a measurement. Protection is on the cell side, so pulling the link never leaves a bare cell.
TP1	TP	TestPoint:TestPoint_Pad_ D1.0mm	- (copper pad, no part fitted)	[S9] VBAT_CELL - cell positive, for Q3.
TP2	TP	TestPoint:TestPoint_Pad_ D1.0mm	- (copper pad, no part fitted)	[S9] VRECT - rectified node, for Q4.
TP3	TP	TestPoint:TestPoint_Pad_ D1.0mm	- (copper pad, no part fitted)	[S9] VBAT - driver supply ahead of the bank, for Q2.
TP4	TP	TestPoint:TestPoint_Pad_ D1.0mm	- (copper pad, no part fitted)	[S9] VDRV - driver supply behind the bank, for Q2. TP3 and TP4 together are how the droop calculation in §5.6 is falsified.
TP5	TP	TestPoint:TestPoint_Pad_ D1.0mm	- (copper pad, no part fitted)	[S9] VDD - controller logic rail. Also the check that UICR REGOUT0 was actually programmed to 3.0 V and the part did not come up at its 1.8 V default.
TP6	TP	TestPoint:TestPoint_Pad_ D1.0mm	- (copper pad, no part fitted)	[S9] TCH_CHANGE - touch interrupt, for Q1.
TP7	TP	TestPoint:TestPoint_Pad_ D1.0mm	- (copper pad, no part fitted)	[S9] ACC_INT - accelerometer interrupt. Q1 is a question about TP6 and TP7 agreeing.
TP8	TP	TestPoint:TestPoint_Pad_ D1.0mm	- (copper pad, no part fitted)	[S9] GND, first of two.
TP9	TP	TestPoint:TestPoint_Pad_ D1.0mm	- (copper pad, no part fitted)	[S9] GND, second of two, **physically separated from TP8**. Not redundancy: a long ground lead is how a 20 ms haptic droop measurement acquires 200 mV of ringing that is not there.

Refdes	Value	Footprint	MPN	Rationale
H1	M2	MountingHole:MountingHole_2.2mm_M2	- (mechanical, no part fitted)	[S0] Mounting hole for the printed wear-test carrier.
H2	M2	MountingHole:MountingHole_2.2mm_M2	- (mechanical, no part fitted)	[S0] Second mounting hole; two holes fix rotation so the electrode flex leaves in a repeatable direction.

90 refdes. Ceiling is 105 placed symbols (`parts.symbol_ceiling`), so headroom is **15**, better than the 5 the architecture stage allocated - the controller decoupling came in under its allocation. `J2` is deliberately unused: SPEC §2.1 names J1 and J3–J8 and the numbering is kept faithful to it rather than renumbered.

Footprint identifiers above are provisional. Stage 4 needs only the symbols in §3; footprints are confirmed against the installed footprint libraries at layout stage.

---

2. Quiescent / leakage check against the power budget

Every part that can draw current when the ring is idle and off the dock, checked against its subsystem allocation in `docs/SUBSYSTEMS.md` §4.

Refdes	Idle draw from the cell	Allocation	Verdict
U1	3.2 μA System ON + 1.5 μA CPU wake + 22.0 μA radio	S4 4.8, S5 22.0	within, **before** the REG0-LDO penalty in §4.2
U2	40.0 μA LP burst, 128 ms, 7 keys	S6 40.0	at allocation; pessimistic - only 5 keys are fitted
U3	8.7 μA wake-up engine, 12.5 Hz	S7 8.7	at allocation
U4	1.0 μA max, EN held low by R20	S8 (part of 6.4)	within
U5	2.0 μA battery drain, V_DD unpowered	S2 2.0	at allocation, **A22 - measure on J7**
U6	3.0 μA typ, 6.0 μA max	S1 3.0	at typ; the max would consume 3 μA of contingency
Q1	< 0.1 μA gate leakage, enhanced on	S1	negligible
D2, D3	~0 at 0 V reverse bias off-dock	S3 0.5 (allowance)	within
D4	0 - VRECT is 0 V off-dock, the Zener is not biased	S3	zero by placement
D1, R4	0 - lit only on the dock	S2	outside the discharge duty cycle
R5, R6	0 from the cell; 25.5 μA from the **dock**	S2	zero by placement
R7, R8	0 from the cell; 3.5 μA from the **dock**	S3	zero by placement - this is why the divider is on VRECT, not VBAT
R9, R10, R11, R17, R18	0.1 μA total, lines idle high	S4/S6 0.1	within
R20	0.03 μA when HAP_EN is driven high, else 0	S8	negligible
C31–C34	**~4.0 μA** typical (1 μA/part)	S8 - **overspend**	see §4.1
All other ceramics	included in the 2.0 μA board-wide allowance	S0 2.0	within

Revised totals. Itemised sub-total **89.4** → **96.9 µA** (+4.0 µA bank leakage, +3.5 µA REG0-as-LDO). With the 20 % contingency: **116.3 µA**.

Against	Value	Margin	Verdict
`power.average_target_uA` 150	116.3	33.7 µA (22 %)	**within**
`power.average_ceiling_uA` 177	116.3	60.7 µA (34 %)	**within**
`power.budget_total_uA` 107.3	116.3	**−9.0 µA**	**exceeded** - see §4.4

Predicted endurance at 116.3 µA: 17 mAh ÷ 116.3 µA = **146 h ≈ 6.1 days**, still well past the 96 h bar.

---

3. Symbol map - machine-confirmed on this machine

Stage 4 draws only from these. Each lib_id was returned by `search_symbols` and its pins read back with `symbol_pins` in this run.

Refdes	lib_id	Pins confirmed
U1	`MCU_Nordic:nRF52833_QDxx`	41, 1 unit
U2	`Sensor_Touch:AT42QT1070-M`	21, 1 unit
U3	`Sensor_Motion:KX022-1020`	11, 1 unit
U4	`Driver:DRV2605LDGS`	10, 1 unit
U5	`Battery_Management:MCP73831-2-OT`	5, 1 unit
U6	`Battery_Management:AP9101CK6`	6, 1 unit
Q1	`Transistor_FET:Q_Dual_NMOS_S1G1D2S2G2D1`	6, **2 units** - engine places each unit under the one refdes
D1	`Device:LED`	2
D2, D3	`Diode:BAT54S`	3 (A, K, COM)
D4	`Device:D_Zener`	2
Y1	`Device:Crystal_GND24`	4
Y2	`Device:Crystal`	2
L1, L2	`Device:L`	2
ANT1	`Device:Antenna_Chip`	2 (FEED, PCB_Trace)
R1–R20	`Device:R`	2
C1–C36	`Device:C`	2
J1	`Connector_Generic:Conn_02x05_Odd_Even`	10
J4	`Connector_Generic:Conn_01x06`	6
J3, J5, J6, J7, J8	`Connector_Generic:Conn_01x02`	2
TP1–TP9	`Connector:TestPoint`	1
H1, H2	`Mechanical:MountingHole`	0

Symbols that do not exist on this machine and were therefore not used: `DMN65D8LDW` (no match in any installed library - the dual protection FET is captured with the generic `Transistor_FET:Q_Dual_NMOS_S1G1D2S2G2D1` and the MPN carried in the BOM row instead), and `Sensor_Motion:LIS2DH12TR` (the installed name is `Sensor_Motion:LIS2DH`; not needed, the KX022-1020 symbol exists).

3.1 Hard strap pins - these are not GPIO

Part	Pin	Tie	Consequence of getting it wrong
U2	MODE (11)	**VSS**	High selects standalone-output mode; the part would never answer on I^2C
U2	~RESET (13)	10 k to VDD (R18)	Floating reset gives an intermittently dead touch controller
U3	~CS (10)	**IO_VDD**	Low selects SPI; the part is present, powered and silent on the bus
U3	SDO/ADDR (1)	**GND**	Selects 0x1E; tied high it collides with nothing but firmware looks at the wrong address
U3	TRIG (4)	GND	Unused trigger input must not float
U4	IN/TRIG (4)	GND	Selects I^2C mode over PWM/analog input
U1	P0.09/P0.10	left at NFC default	UICR `NFCPINS`; assigning GPIO here breaks pairing
U1	P0.18	nRESET, R9 pull-up	UICR `PSELRESET`
U1	P0.00/P0.01	XL1/XL2 only	Not available as GPIO
U1	VBUS (10)	**GND**	USB unused; DECUSB (11) left unconnected per Nordic guidance - no parts required, and this absence is deliberate
U1	VRECT_ SENSE	AIN2 / P0.04	Must be one of AIN0–AIN7; A18

---

4. Deviations from SPEC - recorded, not hidden

4.1 Deviation 1 - the haptic bank is 4 × 220 µF MLCC, not 2 × 680 µF polymer

SPEC §5.6 sizes the bank at ≥ 1213 µF and fits 1360 µF as two 680 µF polymer aluminium parts. That part class cannot be reconciled with a single-digit-µA idle budget: polymer aluminium capacitors specify leakage in the tens to hundreds of microamps at rated voltage, which on this board would be the largest line in the table by a wide margin. There is no polymer part that is both 680 µF and quiet enough.

Fitted instead: C31–C34, four 220 µF 6.3 V X6S 1210 MLCC.

```
nominal                4 x 220 uF                 = 880 uF
DC-bias derating at 3.7 V, ASSUMED 65 % (A23)     -> ~77 uF each
effective bank                                     ~= 308 uF
allowed droop          deltaV = 3.5 - 2.7              = 0.8 V
charge available       Q = 308 uF x 0.8 V          = 246 uC
over a 10 ms start     I_bank = 246 uC / 10 ms     = 24.6 mA
plus R_HAP contribution 0.8 V / 15 ohm               = 53 mA
peak the rail supports                             ~= 78 mA
```

78 mA, not the 150 mA of ASSUMED A5. Consequences, all recorded:

- Firmware **must** cap the DRV2605L rated-voltage and overdrive-clamp registers so the actuator start current stays under ~78 mA, until O1 closes with a measured actuator.
- The 150 mA / 10 ms figure was never a datasheet number - it is A5, a typical-coin-LRA assumption. The honest position is that the bank is sized against an assumption either way; this version is sized against an assumption **and** is quiet.

- Leakage: budgeted **1 µA per part, 4.0 µA total**, which is typical for a large X6S at 3.7 V. The datasheet insulation-resistance *limit* is far worse - an IR spec of 50 Ω·F gives 227 kΩ at 220 µF, i.e. 16 µA per part, 65 µA for the bank, which alone would breach the ceiling. **This must be measured on J7 on the first assembled boards**, per lot. Recorded as open item O9.
- Each capacitor has its own refdes so the bank can be depopulated one part at a time on the bench.

Also found while checking this: at the 55 mA steady drive of A6, the drop across R19 is 0.83 V, so at the 3.5 V haptic-inhibit threshold (A8) VDRV = 2.67 V - 30 mV **below** the 2.7 V floor of A9. SPEC §5.6 mixes a 53 mA droop calculation with a 55 mA drive current and does not notice. Fix is firmware, not parts: raise the inhibit threshold to 3.6 V, or cap the drive at 50 mA. Recorded as open item O11.

4.2 Deviation 2 - REG0 runs as an LDO; there is no VDDH buck inductor

The installed `MCU_Nordic:nRF52833_QDxx` symbol exposes **DEC4 (38) and DCC (39) but no DCCH**. The REG0 high-voltage buck needs an inductor from DCCH to VDD, and a pin that does not exist in the symbol cannot be wired in stage 4. **The REG1 buck is unaffected** - L1 sits between DCC and DEC4 as normal, so the 22 µA radio row keeps its DC/DC assumption.

Cost of running REG0 as an LDO instead of a buck:

```
VDD-side load        U2 40.0 + U3 8.7 + U1 core 4.7 + radio 22.0 + pull-ups 0.1 = 75.5 uA
with REG0 buck (85%) I_cell = 75.5 x 3.0 / (3.7 x 0.85) = 0.954 x 75.5 = 72.0 uA
with REG0 as LDO     I_cell = 75.5 uA
penalty                                                                  = +3.5 uA
```

+3.5 µA, 2.3 % of the 150 µA target. The high-voltage buck was never worth much here because the step from 3.7 V to 3.0 V is small; the part was chosen for VDDH's 5.5 V tolerance, not for REG0's efficiency, and that reason is untouched. Recorded as ASSUMED A24 and open item O10 - if a later KiCad symbol exposes DCCH, add one 10 µH inductor and recover 3.5 µA.

4.3 Deviation 3 - CHG_STAT needs a level shift

MCP73831 STAT is a **push-pull** output referenced to its own V_DD, which here is VRECT at 5.1 V nominal and 5.4 V at the clamp maximum. Wired straight to a GPIO it exceeds the SoC's VDD + 0.3 V = 3.3 V absolute maximum. SPEC §3.2/§10 and SUBSYSTEMS §3.2 both describe a pull-up, which is the wiring for an open-drain status pin this part does not have.

Fitted: R5/R6, a 100 k / 100 k divider from STAT to GND with the GPIO on the tap.

```
tap at VRECT 5.1 V nominal   = 2.55 V   (logic high at 3.0 V VDD [x])
tap at VRECT 5.4 V clamp max = 2.70 V   (< 3.3 V absolute max [x])
tap with STAT low            = 0 V
tap off-dock, charger unpowered = 0 V, held by R6 - no floating GPIO
divider current              = 5.1 V / 200 kohm = 25.5 uA, drawn from the DOCK
```

Zero cost to the cell budget, because it hangs off VRECT which is 0 V off the dock - the same placement argument that put the sense divider on VRECT rather than VBAT. A single N-FET plus pull-up was the alternative; two resistors were chosen because they add the same symbol count, cannot be fitted the wrong way round, and do not invert the sense of the signal. Recorded as ASSUMED A25.

4.4 The budget bookkeeping figure is exceeded - this needs a human

`power.budget_total_uA` is a **derived** number: the itemised sub-total × 1.2. The two deviations above raise the sub-total from 89.4 to 96.9 µA, so the derived total moves from 107.3 to **116.3 µA**, exceeding the recorded 107.3 by 9.0 µA.

The two product requirements are both still met - 116.3 μA is inside the 150 μA design target with 22 % headroom and inside the 177 μA hard ceiling with 34 %. Nothing in the brief is violated. What is violated is a derived bookkeeping ceiling that was correct for the previous parts list, and two subsystem allocations that must be re-issued:

Subsystem	Allocated	Now	Reason
S4 controller core	4.8 μA	8.3 μA	REG0 as LDO, Deviation 2
S8 haptic	6.4 μA	10.4 μA	MLCC bank leakage, Deviation 1

`docs/SUBSYSTEMS.md` §0 rule 1 requires an overspend to be a transfer from a named donor, not a quiet expansion. **There is no donor with slack**: every other subsystem is at its allocation. So this is not a transfer, it is a genuine increase in the itemised total, charged against the margin that exists between 107.3 μA and the 150 μA target. Recorded in `docs/DECISIONS.md` as an open item for the human, who may instead choose to (a) fund it from the 128 ms touch scan interval, which SPEC §4.3 already names as the first knob (256 ms roughly halves 40 μA), or (b) accept the increase, which is what this document proposes.

---

5. Rules checked across the whole BOM

Privacy (`privacy.forbidden_parts`). No microphone, camera, photoplethysmography or optical heart-rate part, skin-contact electrode, temperature sensor, skin-impedance sensor, speaker or bone-conduction transducer appears anywhere above. The only sensors on the board are a capacitive touch controller and an accelerometer used as an interlock; the only output is an LRA. Kyra R1 is a control device, not a capture device, and this list is the enforcement.

Forbidden blocks (`arch.forbidden_blocks`). No external flash, no battery-sense divider on VBAT, no external regulator on the logic rail, no gyroscope, no magnetometer, no second MCU, no low-frequency wireless-power receiver IC, no transmitter or dock circuitry. Each absence is deliberate and is listed in `docs/SUBSYSTEMS.md` §8. The charge LED (D1, R4) is present on EV1 and explicitly **not** in the ring build.

Environment (`env.operating_C` 0…+45, `env.storage_C` −20…+60). All ceramics are C0G, X5R, X6S or X7R (−55/+85 °C or better); both crystals are specified −40/+85 °C; every IC is industrial grade; the JST SH connectors are −25/+85 °C, which covers the −20 °C storage floor. No part rated 0/+70 °C is used.

Passive size (`parts.min_passive_size`). 0402 is the smallest package on the board. Larger sizes are used only where voltage rating, capacitance or dissipation demands it: 0603 for 4.7 μF bulk, 0805 for R19 and the 10 μF/4.7 μF 16 V parts, 1210 for the haptic bank.

I²C addresses (`i2c.addresses`). 0x1B (U2, fixed), 0x1E (U3, ADDR to GND), 0x5A (U4, fixed). No collision. Bus pull-ups fitted once, in S4, at 4.7 kΩ.

Symbol ceiling (`parts.symbol_ceiling`). 90 placed symbols against a ceiling of 105.

---

6. Open items introduced by this stage

#	Item	Blocks
O9	Haptic bank leakage is budgeted at 1 μA/part typical while the MLCC insulation-resistance limit implies up to 16 μA/part. Must be measured on J7 per lot.	§4.1, the whole current budget
O10	The installed nRF52833 symbol has no DCCH pin, so REG0 runs as an LDO and costs 3.5 μA. Revisit if a later symbol exposes it.	§4.2
O11	At 55 mA drive (A6) the R19 drop puts VDRV 30 mV below the 2.7 V floor (A9) at the 3.5 V inhibit threshold (A8). Raise the threshold to 3.6 V or cap drive at 50 mA.	§4.1, SPEC §5.6

PART V

DECISIONS

Source: docs/DECISIONS.md

- 2026-09-01 [run 2026-09-01T21-22-18-951Z] Logic rail VDD = 3.0 V from the nRF52833 internal REG0 (ASSUMED A1); no external regulator anywhere on the board | why: 3.0 V is inside the KX022-1020 3.6 V maximum and well above the AT42QT1070 1.8 V minimum, and gives faster I2C edges than the 1.8 V REG0 default; the cell goes to VDDH (1.8-5.5 V) directly, which is the entire reason the nRF52833 was chosen over the nRF52832. Carries a firmware obligation: UICR REGOUT0 must be programmed to 3.0 V, because a blank part comes up at 1.8 V. | affects: VDD net, U1 nRF52833, U2 AT42QT1070, U3 KX022-1020, I2C pull-ups, docs/SPEC.md §3.3/§5.7/§12
- 2026-09-01 [run 2026-09-01T21-22-18-951Z] Haptic series element is a 15 ohm resistor, not a ferrite bead, feeding a 2 x 680 uF polymer bank (1360 uF) on VDRV | why: KYR-404 permits either, but a bead is ~0 ohm at DC and would not bound the cell's current at all; the DC resistance is the whole mechanism. 15 ohm caps the cell at 53 mA under the 0.8 V droop budget, inside the 60 mA (3C) limit, and 1360 uF holds the 97 mA start excess for 10 ms with 0.71 V actual droop. Derived firmware constraint: >=150 ms pulse spacing for bank recharge (tau = 20.4 ms). | affects: VDRV, VBAT, R_HAP, C_BANK1/2, U4 DRV2605L, docs/SPEC.md §5.6, §4.4
- 2026-09-01 [run 2026-09-01T21-22-18-951Z] The VRECT_SENSE divider (1 M / 470 k) sits on the rectified node, not on VBAT, and is the only divider on the board | why: KYR-605 requires the sense for Q4 and decision 8 deletes the battery-sense divider. Placing it on VRECT means it draws zero from the cell off the dock (VRECT = 0 V) instead of 2.5 uA continuously, which would have been 1.7% of the 150 uA target for a measurement only needed while docked. Carries a firmware obligation: 320 kOhm source impedance needs SAADC T_ACQ >= 20 us, not the 10 us default. | affects: VRECT_SENSE net, R_TOP/R_BOT, U1 AIN2 (P0.04), docs/SPEC.md §5.9, §4.2
- 2026-09-01 [run 2026-09-01T21-22-18-951Z] Electrode series resistors fixed at 1 kohm 0402 on all five electrode lines, at the low end of the 1k-10k QTouch range | why: KYR-204 requires the value to be a recorded decision. 1 kohm gives ESD/EMI limiting on lines that leave the board on a flex tail while keeping RC <= 20 ns against 5-20 pF electrodes, which is negligible against microsecond-scale charge-transfer bursts; the low end is chosen because the flex leads are long and extra series resistance costs sensitivity, which Q1 cannot afford. Tuning range 470 ohm - 4.7 k. | affects: E_STRIP1..3, E_GUARD, E_WEAR, U2 AT42QT1070, J4 FFC, docs/SPEC.md §5.8
- 2026-09-01 [run 2026-09-01T21-22-18-951Z] Clamp on VRECT set to 5.1 V +/-5% (500 mW, ASSUMED A12), inside a derived 4.5-6.0 V window | why: Window is derived, not chosen: lower bound is VBAT_max 4.2 V plus 0.3 V charger dropout margin; upper bound is the MCP73831 7 V absolute-maximum input minus a 1 V design margin. 5.1 V is inside it at both tolerance extremes (4.85 V / 5.36 V) and is also what makes the KYR-505 thermal check trivial - a 6.8 V clamp would raise charger dissipation from 38 mW to 63 mW. Clamp power rating stays ASSUMED because the dock's delivered power is out of scope (KYR-606). | affects: VRECT, D_CLAMP, C_RECT, U5 MCP73831, docs/SPEC.md §5.3, §5.2
- 2026-09-01 [run 2026-09-01T21-47-38-127Z] The board is partitioned into ten ownership domains S0-S9 (board-wide, cell/protection, charging, wireless receive, controller core, connectivity, thumb interface, motion interlock, haptic, instrumentation). Each domain owns its nets, a hard share of the 89.4 uA itemised sub-total and a symbol allocation; the 20% contingency (17.9 uA) is board-wide and belongs to no subsystem. | why: SPEC.md is organised by requirement id and by calculation, which answers 'is this value correct' but not 'whose budget is this'. Capture and layout need the second answer: without owned shares, an increase anywhere silently spends someone else's margin and the first sign is a board that misses 177 uA on the bench. Making allocation a ceiling rather than a forecast means an overspend requires an explicit recorded transfer with both sides named,

and making the contingency unallocated stops it being quietly consumed as 'available headroom' by whichever subsystem grows first. | affects: docs/SUBSYSTEMS.md (new, all sections), docs/SPEC.md §4.2 partition, all later capture/layout stages

- 2026-09-01 [run 2026-09-01T21-47-38-127Z] Electrode series resistors reduced from six to five (E_STRIP1..3, E_GUARD, E_WEAR); J4's sixth way is the flex ground return and deliberately carries no series resistor. | why: SPEC §5.8 and §3.7 said six series resistors while the canonical net list in §3.4 names only five electrode nets - the sixth way of the 6-way FFC is the flex ground/shield return. Putting a resistor in a shield return defeats the shield it exists to provide, so the absence is deliberate and is recorded here so a reviewer does not read the missing sixth resistor as a capture omission. Recorded as open item O8; closes with the electrode geometry (O5). | affects: docs/SPEC.md §3.7/§5.8/§13, docs/SUBSYSTEMS.md §3.6/§8/§9, S6 thumb interface, J4, U2 AT42QT1070, symbol count
- 2026-09-01 [run 2026-09-01T21-47-38-127Z] Recorded worst-case placed-symbol count as 100 against the 105 ceiling - real headroom is 5 symbols, not the ~13 the previous "92-98" estimate implied. If the count approaches 105 the reduction comes out of S4 (controller) decoupling multiplicity, never out of S9 (instrumentation). | why: SPEC §3.7's per-block rows sum to 101 as written (100 after the electrode-resistor reconciliation) while the stated total was a "~92-98" range that was never checked against its own table. A stage that plans to 'add a couple of parts' against 13 phantom symbols of slack will breach parts.symbol_ceiling during capture, when removing parts is most expensive. Naming S4 decoupling as the designated donor and S9 as untouchable encodes SPEC §2.3's rule - the board exists to be measured, so instrumentation is the last thing cut. | affects: docs/SPEC.md §2.3/§3.7, docs/SUBSYSTEMS.md §5, .copperhead/constraints.json parts.symbol_ceiling, capture stage
- 2026-09-02 [run 2026-09-02T00-41-49-312Z] Haptic bank fitted as C31-C34, 4 x 220 uF 6.3 V X6S 1210 MLCC (880 uF nominal, ~308 uF effective after 65% DC-bias derating at 3.7 V), replacing the 2 x 680 uF polymer aluminium bank of SPEC §5.6. OPEN ITEM FOR HUMAN: the rail then supports ~78 mA of start current, not the 150 mA of ASSUMED A5, so firmware must cap the DRV2605L overdrive registers until O1 closes. | why: Polymer aluminium specifies leakage in the tens to hundreds of microamps at rated voltage; on a board whose entire itemised budget is 89.4 uA that class is unbuyable, and no polymer part is both 680 uF and quiet enough. The trade is capacitance for quiet, and it is defensible because the 150 mA/10 ms figure it fails to meet was never a datasheet number - it is assumption A5 - so the bank is sized against an assumption either way; this version is sized against an assumption and is also silent. Each cap gets its own refdes so the bank can be depopulated one part at a time on the bench. Leakage budgeted at 1 uA/part (A27); the MLCC insulation-resistance limit implies up to 16 uA/part, which alone would breach the ceiling, hence open item O9 requiring a J7 measurement per lot. | affects: C31, C32, C33, C34, VDRV, U4 DRV2605L, S8 allocation 6.4 -> 10.4 uA, docs/BOM.md §4.1, docs/SPEC.md §5.6/§4.2/§12/§13, docs/SUBSYSTEMS.md §2/§3.8/§4
- 2026-09-02 [run 2026-09-02T00-41-49-312Z] REG0 runs as an LDO: no VDDH buck inductor is fitted, because the nRF52833 symbol installed on this machine exposes DEC4 (38) and DCC (39) but no DCCH pin. The REG1 buck is unaffected (L1 10 uH between DCC and DEC4), so the 22 uA radio row keeps its DC/DC assumption. OPEN ITEM FOR HUMAN: this costs +3.5 uA and is recoverable with one inductor if a later KiCad symbol exposes DCCH (open item O10). | why: A pin that does not exist in the installed symbol cannot be wired at stage 4, and stage 4 draws only from installed symbols; substituting a different SoC to recover 3.5 uA would discard the VDDH 1.8-5.5 V tolerance that is the entire reason this part was chosen over the nRF52832. The penalty is bounded and computed, not guessed: 75.5 uA of VDD-side load at 3.0 V costs 72.0 uA from a 3.7 V cell through an 85%-efficient buck versus 75.5 uA through an LDO, so +3.5 uA, 2.3% of the 150 uA target. The step from 3.7 V to 3.0 V is small, which is why the high-voltage buck was never worth much here. | affects: U1 nRF52833, L1, C13, C21, VDD, VDDH, S4 allocation 4.8 -> 8.3 uA, docs/BOM.md §4.2, docs/SPEC.md §4.2/§12 A24/§13 O10, docs/SUBSYSTEMS.md §3.4
- 2026-09-02 [run 2026-09-02T00-41-49-312Z] CHG_STAT is level-shifted to the SoC GPIO by R5/R6, a 100k/100k divider from the MCP73831 STAT pin to GND with the tap on the GPIO - not by the pull-up that SPEC §3.2/§10 and SUBSYSTEMS §3.2 previously described. | why: The MCP73831 STAT output is push-pull referenced to its own V_DD, which on this board is VRECT at 5.1 V nominal and 5.4 V at the clamp maximum; wired directly it exceeds the SoC's VDD+0.3 V = 3.3 V absolute maximum, and a pull-up is the wiring for an open-drain pin this part does not have. The divider gives 2.55 V at nominal VRECT and 2.70 V at clamp max (both a valid logic high on a 3.0 V rail, both under the absolute maximum), and the bottom resistor defines the

GPIO as low when the charger is unpowered off-dock, so the input never floats. Its 25.5 uA is drawn from the dock and never from the cell - the same placement argument that put the sense divider on VRECT rather than VBAT. Two resistors were chosen over an N-FET plus pull-up because they cost the same symbol count, cannot be fitted the wrong way round, and do not invert the sense of the signal. | affects: R5, R6, CHG_STAT, U5 MCP73831-2-OT, U1 GPIO, docs/BOM.md §4.3, docs/SPEC.md §12 A25, docs/SUBSYSTEMS.md §3.2

- 2026-09-02 [run 2026-09-02T00-41-49-312Z] OPEN ITEM FOR HUMAN - the derived power.budget_total_uA bookkeeping figure of 107.3 uA is exceeded. Part selection moves the itemised sub-total 89.4 -> 96.9 uA (+4.0 uA MLCC bank leakage in S8, +3.5 uA REG0-as-LDO in S4), so the x1.2 total becomes 116.3 uA, 9.0 uA over the recorded ceiling. Proposed resolution: accept the increase. Alternative resolution if the human prefers to stay under 107.3: move the AT42QT1070 LP scan interval from 128 ms to 256 ms, which SPEC §4.3 already names as the first knob and which recovers ~20 uA at the cost of gesture latency. | why: Both product requirements still hold with room: 116.3 uA is inside the 150 uA design target by 33.7 uA (22%) and inside the 177 uA hard ceiling by 60.7 uA (34%), giving 146 h predicted endurance against a 96 h bar. What is breached is a derived bookkeeping number that was correct for the previous parts list, not a brief requirement. SUBSYSTEMS §0 rule 1 requires an overspend to be an explicit transfer naming a donor, and there is no donor: every other subsystem sits exactly at its allocation. So this is recorded as a genuine increase charged against target margin rather than dressed up as a transfer, and it is flagged for the human because re-issuing two subsystem allocations is not a decision the part-selection stage owns alone. | affects: .copperhead/constraints.json power.budget_total_uA and power.subsystem_allocation_uA, S4 4.8 -> 8.3 uA, S8 6.4 -> 10.4 uA, docs/BOM.md §2/§4.4, docs/SPEC.md §4.2, docs/SUBSYSTEMS.md §2/§4

PART VI

Design changelog

Source: docs/CHANGELOG.md

Append-only, newest first. One entry per committed copperhead run.

2026-09-02 - create pipeline stage: part-selection

- Change: part-selection-bom-ev1
- Files: docs/BOM.md, docs/SPEC.md, docs/SUBSYSTEMS.md, docs/DECISIONS.md, docs/CHANGELOG.md
- Verification: ERC not required

2026-09-02 - create pipeline stage: part-selection

- Change: part-selection-bom-ev1
- Files: docs/BOM.md (new), docs/SPEC.md (§3.2 AP9101CK6, §3.6 DCCH row, §4.2 delta, §5.6 superseded bank, §12 A23–A27, §13 O9–O11), docs/SUBSYSTEMS.md (§2, §3.2, §3.4, §3.8, §4, §9), docs/DECISIONS.md, docs/CHANGELOG.md
- Summary: 90-row bill of materials, one row per refdes, every active symbol confirmed installed on this machine with search_symbols + symbol_pins. Three SPEC values could not be realised as written and are recorded as deviations rather than refusals: the 2 × 680 μF polymer haptic bank became 4 × 220 μF MLCC (polymer leaks tens–hundreds of μA against an 89.4 μA budget; ~308 μF effective supports ~78 mA start, not A5's 150 mA); REG0 runs as an LDO because the installed nRF52833 symbol has no DCCH pin (+3.5 μA); CHG_STAT gained a 100 k/100 k level shift because MCP73831 STAT is push-pull to VRECT, not open-drain. Itemised sub-total 89.4 → 96.9 μA, budget total 107.3 → 116.3 μA - inside the 150 μA target and the 177 μA ceiling, over the derived bookkeeping figure, flagged as an open item for the human. Also found: at A6's 55 mA drive, VDRV sits 30 mV below the A9 floor at the A8 inhibit threshold (O11).
- Verification: ERC not required (no schematic yet); check_drift clean

2026-09-01 - create pipeline stage: architecture

- Change: architecture-subsystem-decomposition
- Files: docs/SUBSYSTEMS.md, docs/SPEC.md, docs/CHANGELOG.md, docs/DECISIONS.md
- Verification: ERC not required

2026-09-02 - create pipeline stage: architecture

- Change: architecture-subsystem-decomposition
- Files: docs/SUBSYSTEMS.md (new), docs/SPEC.md (§2.3 parts budget, §3.7 symbol table, §5.8 electrode resistors, §13 open item O8), docs/DECISIONS.md, docs/CHANGELOG.md
- Summary: partitioned the board into ten ownership domains (S0–S9), each owning its nets, its share of the 89.4 uA itemised sub-total and its symbol count; added an interface contract with one producer per net, a cross-domain hazard list, and a deliberate-absences table. Two arithmetic reconciliations against SPEC: worst-case

symbol count is 100 (headroom 5, not 13), and electrode series resistors are five, not six (O8).

- Verification: ERC not required (no schematic yet); check_drift clean

2026-09-01 - create pipeline stage: spec-seed

- Change: seed-kyra-r1-ev1-requirements
- Files: docs/SPEC.md, openspec/specs/controller-radio/spec.md, openspec/specs/thumb-interface/spec.md, openspec/specs/motion-interlock/spec.md, openspec/specs/haptic-escalation/spec.md, openspec/specs/cell-charging/spec.md, openspec/specs/wireless-receive/spec.md, openspec/specs/pairing-identity/spec.md, openspec/specs/instrumentation/spec.md, openspec/specs/power-budget/spec.md, docs/DECISIONS.md
- Verification: ERC not required

PART VII

Capability: Cell, Protection and Charging

Source: openspec/specs/cell-charging/spec.md

Source requirements: KYR-501 … KYR-505 (`brief.md` §5). Budgets in `docs/SPEC.md` §5.1, §5.2.

ADDED Requirements

Requirement: Single curved Li-Po cell on a two-way connector

The board SHALL take a single curved lithium-polymer cell, **20 mAh nominal, 3.7 V**, on a two-way connector so cells can be swapped during the power study. It is a **bare cell with no protection module of its own**. (KYR-501)

Scenario: Cells are swapped during the power study

- **GIVEN** Q3 requires measuring average current against real cells
- **WHEN** a different cell is fitted to J5
- **THEN** no board change is required

Scenario: The cell arrives unprotected

- **GIVEN** the cell has no protection module
- **WHEN** the cell is connected
- **THEN** the board's own protection network is the only protection present, so it SHALL be populated on every build

Requirement: Discrete cell protection on the board

The board SHALL implement discrete cell protection - over-charge, over-discharge and over-current - using a protection controller and a **common-source pair of low on-resistance N-channel MOSFETs in the cell's negative leg** (`Battery_Management:AP9101CK` class). This is **non-negotiable**: a bare pouch cell in a sealed product worn on a finger has no other protection. (KYR-502)

Scenario: Over-discharge

- **GIVEN** the cell falls below the controller's over-discharge threshold
- **WHEN** the protection controller trips
- **THEN** it turns off the discharge FET in the `CELL_NEG` leg and isolates the load

Scenario: Over-charge

- **GIVEN** the charger or a fault pushes the cell above the over-charge threshold
- **WHEN** the protection controller trips
- **THEN** it turns off the charge FET, and the body diode of the discharge FET still allows the load to run

Scenario: Protection stays attached while current is measured

- **GIVEN** KYR-802 puts a jumper in the cell's positive leg

- **WHEN** J7 is removed and replaced by a meter
- **THEN** the protection network remains connected on the cell side of J7, so the cell is never unprotected during the measurement

Scenario: Removing protection is proposed to save parts

- **GIVEN** the symbol budget is tight
- **WHEN** a change proposes deleting the protection block
- **THEN** the change is rejected: KYR-502 is non-negotiable

Requirement: Linear charge controller programmed for 15 mA

The board SHALL use a linear charge-management controller programmable to the low current a 20 mAh cell needs (`Battery_Management:MCP73831-2-OT`), programmed for **15 mA**, with the resistor its datasheet's programming equation gives. Both the resistor and the equation SHALL be stated. (KYR-503)

Scenario: The programming resistor is derived, not guessed

- **GIVEN** the datasheet equation I_REG = 1000 V / R_PROG
- **WHEN** 15 mA is required
- **THEN** R_PROG = 1000 / 0.015 = 66.67 kΩ, fitted as **66.5 kΩ 1 % 0402 (E96)**
- **AND** the realised current is 1000 / 66 500 = 15.04 mA

Scenario: Charge time meets the category expectation

- **GIVEN** 15 mA into a 20 mAh cell is 0.75 C
- **WHEN** the cell is charged from empty
- **THEN** it fills in about 1.6 h

Scenario: The cell turns out to be a 0.5 C part

- **GIVEN** open item O2 leaves the cell's permitted charge rate unknown
- **WHEN** the cell is confirmed as 0.5 C
- **THEN** 10 mA is required, which is below where this charger regulates accurately, and the **charger changes** to one that regulates accurately at 10 mA

Scenario: Accuracy at the bottom of the range is acknowledged

- **GIVEN** 15 mA is the bottom of the MCP73831's programmable range
- **WHEN** the charge current is specified
- **THEN** ±10 % accuracy is recorded as ASSUMED (A20) rather than claimed as exact

Requirement: Charge-status output to controller and LED

The charge-status output SHALL go to the controller, so the ring knows it is on the dock, **and** to the single instrumentation LED. (KYR-504, KYR-804, decision 6)

Scenario: The ring knows it is docked

- **GIVEN** `CHG_STAT` is connected to a SoC GPIO
- **WHEN** charging begins
- **THEN** firmware can suppress escalations or change behaviour while docked

Scenario: The LED is not in the ring build

- **GIVEN** an indicator on your hand is a notification other people can read
- **WHEN** the production ring is built
- **THEN** the charge-status LED is not fitted; it exists on EV1 only, in the instrumentation block

Scenario: The LED does not spend the discharge budget

- **GIVEN** the LED lights only while charging
- **WHEN** the 96 h discharge budget is computed
- **THEN** the LED contributes zero, and this is stated explicitly rather than omitted

Requirement: Charger thermal check at the clamped rectifier voltage

The specification SHALL state the charger's worst-case dissipation at 15 mA from the clamped rectifier voltage and confirm the package handles it. (KYR-505)

Scenario: Worst-case dissipation is computed

- **GIVEN** the clamp holds the input at 5.4 V worst case and the cell is at 2.9 V in CC
- **WHEN** dissipation is computed
- **THEN** P_D = $(5.4 - 2.9) \times 0.015$ = **37.5 mW**

Scenario: The package handles it

- **GIVEN** SOT-23-5 with θ_JA $\approx$ 230 °C/W and a 45 °C maximum ambient
- **WHEN** junction temperature is computed
- **THEN** T_j = 45 + 0.038×230 = **53.7 °C**, far below the 150 °C limit
- **AND** the low 5.1 V clamp is what makes this trivial, linking KYR-505 to KYR-604

PART VIII

Capability: Controller and Radio

Source: openspec/specs/controller-radio/spec.md

Source requirements: KYR-101 … KYR-106 (`brief.md` §1). Budgets in `docs/SPEC.md` §3, §4.

ADDED Requirements

Requirement: Multiprotocol BLE SoC in VDDH high-voltage mode

The board SHALL use a multiprotocol Bluetooth Low Energy system-on-chip with an Arm Cortex-M4F and **VDDH high-voltage mode** (1.8 V to 5.5 V), specifically the nRF52833 in QFN-40 (`MCU_Nordic:nRF52833_QDxx`), so the cell connects to it directly. There SHALL be **no external regulator on the logic rail**. (KYR-101)

Scenario: Cell at full charge drives the SoC directly

- **GIVEN** a Li-Po cell at its 4.2 V maximum on net `VBAT`
- **WHEN** `VBAT` is connected to the SoC's `VDDH` pin with no intervening regulator
- **THEN** 4.2 V is inside the 1.8–5.5 V `VDDH` range and the part operates normally
- **AND** the internal REG0 produces `VDD` for the rest of the board

Scenario: The cell is never connected to VDD

- **GIVEN** `VDD` has a 3.6 V absolute maximum
- **WHEN** any net is routed to a `VDD` pin
- **THEN** that net SHALL be the REG0 output and never `VBAT` or `VBAT_CELL`

Scenario: An external logic regulator is proposed

- **GIVEN** KYR-101 forbids a regulator on the logic rail
- **WHEN** a change adds an LDO or DC-DC producing `VDD`
- **THEN** the change is rejected, because deleting that regulator is the stated reason the nRF52833 was chosen over the nRF52832

Requirement: High-voltage supply network per the vendor reference

The board SHALL implement the vendor's high-voltage reference supply network: `VDDH` decoupling, the REG0 output routed to `VDD`, the `DEC4` capacitor, and the `DCC` inductor network for the internal DC-DC converter, with decoupling on **every** `VDD` pin. The internal DC-DC SHALL be usable; a topology that forces LDO-only operation SHALL NOT be populated. (KYR-102)

Scenario: DC-DC network is populated

- **GIVEN** the internal DC-DC must be usable
- **WHEN** the supply network is captured
- **THEN** `DCC`, `DCCH` and `DEC4` carry their reference-design inductors and capacitors
- **AND** the 22 μA BLE row of the current budget, which assumes DC-DC on, remains valid

Scenario: Every VDD pin is decoupled

- **GIVEN** the SoC has multiple `VDD` pins
- **WHEN** ERC and the layout review run
- **THEN** each `VDD` pin has its own decoupling capacitor

Requirement: Crystals for radio and real-time counter

The board SHALL carry a 32 MHz crystal with its load capacitors meeting the vendor's BLE frequency tolerance, and a 32.768 kHz crystal with its load capacitors for the real-time counter, because the ring keeps time between connections. (KYR-103)

Scenario: BLE frequency tolerance is met

- **GIVEN** Nordic requires $\leq \pm 40$ ppm total for BLE
- **WHEN** the 32 MHz crystal is selected
- **THEN** its tolerance is ± 20 ppm (ASSUMED A16), leaving margin for ageing and 0–45 °C

Scenario: Ring keeps time between connections

- **GIVEN** the ring must maintain the RTC while disconnected
- **WHEN** the SoC is in System ON with the radio idle
- **THEN** the 32.768 kHz LFXO runs, and its contribution is inside the 3.2 μA System ON row

Scenario: Crystal pins are not reused as GPIO

- **GIVEN** P0.00 and P0.01 are `XL1/XL2`
- **WHEN** GPIO is allocated
- **THEN** P0.00 and P0.01 are excluded from the assignable pool

Requirement: 2.4 GHz chip antenna with a three-element pi match

The board SHALL carry a 2.4 GHz chip antenna fed by a three-element pi matching network on a 50 Ω controlled-impedance path from the radio pin. **All three pi positions SHALL be populated** as placeholders so the network can be tuned on the bench. (KYR-104)

Scenario: Bench tuning without a board spin

- **GIVEN** the production ring will use a printed antenna whose match is re-derived
- **WHEN** EV1 is built
- **THEN** all three pi positions carry parts (0.5 pF / 1.0 nH / 0.5 pF, ASSUMED A17)
- **AND** any of the three can be changed by rework to re-tune the match

Scenario: Controlled impedance from the radio pin

- **GIVEN** the antenna path must be 50 Ω
- **WHEN** the board is laid out
- **THEN** the trace from the `ANT` pin through the pi network is a controlled-impedance 50 Ω line with a continuous reference

Requirement: Reset provision with a pull-up

The board SHALL provide a reset provision and a pull-up on the reset pin. (KYR-105)

Scenario: Reset defaults are respected

- **GIVEN** P0.18 is the default `nRESET` pin selected by UICR `PSELRESET`
- **WHEN** pins are assigned
- **THEN** P0.18 is used as `nRESET`, carries a 10 kΩ pull-up to `VDD`, and is not assigned to any other function

Scenario: Reset reaches the debugger

- **GIVEN** KYR-801 requires the reset line on the SWD header
- **WHEN** the SWD header is wired
- **THEN** `nRESET` appears on the 2×5 header alongside `SWDIO` and `SWDCLK`

Requirement: Two concurrent links not precluded

The radio SHALL be able to hold **two concurrent links**, to a host and to a head-worn display, without a second radio. This is a firmware and stack requirement; the board's obligation is **not to preclude it**. (KYR-106)

Scenario: No second radio is added

- **GIVEN** two links are a stack capability of the nRF52833
- **WHEN** the architecture is reviewed
- **THEN** exactly one radio is present, and no second transceiver is fitted

Scenario: The power budget accounts for two links

- **GIVEN** the current budget must reflect the product's real duty
- **WHEN** the BLE row is computed
- **THEN** it assumes 2 concurrent links at a 1000 ms connection interval (ASSUMED A2)
- **AND** the connection interval is named as the tuning knob if the measured total exceeds the 177 μA ceiling

PART IX

Capability: Haptic Escalation Channel

Source: openspec/specs/haptic-escalation/spec.md

Source requirements: KYR-401 … KYR-405 (`brief.md` §4). Budgets in `docs/SPEC.md` §4.4, §5.6.

ADDED Requirements

Requirement: LRA driver with automatic resonance tracking

The board SHALL use a linear resonant actuator driver with automatic resonance tracking and an I2C interface (`Driver:DRV2605LDGS`). (KYR-401)

Scenario: A short pulse stays crisp

- **GIVEN** a sub-100 ms pulse must be legible on a finger (Q2)
- **WHEN** the driver runs closed-loop with auto-resonance tracking
- **THEN** the drive frequency follows the actuator's resonance and the pulse stays crisp
- **AND** an open-loop driver, which would blur it, is not acceptable

Scenario: Driver shares the one I2C bus

- **GIVEN** the bus carries the touch controller, accelerometer and haptic driver
- **WHEN** addresses are allocated
- **THEN** the driver answers at 0x5A, which collides with neither 0x1B nor 0x1E

Scenario: Driver is powered from VDRV but addressed from a VDD bus

- **GIVEN** the driver sits on `VDRV` (3.5–4.2 V) and the pull-ups sit on `VDD` (3.0 V)
- **WHEN** the SoC addresses the driver
- **THEN** the 3.0 V bus exceeds the driver's absolute 1.3 V `V_IH`, so the cross-rail connection is valid

Requirement: Driver enable on a GPIO, held low when idle

The driver's enable pin SHALL be on a controller GPIO and SHALL be held low when idle, so the driver contributes nanoamps, not microamps, to the standby budget. (KYR-402)

Scenario: Idle standby current

- **GIVEN** `HAP_EN` is driven low by the SoC whenever no pattern is playing
- **WHEN** the current budget is itemised
- **THEN** the driver's row is its shutdown current (1.0 μA datasheet max), not its active or standby current

Scenario: Enable is not tied high

- **GIVEN** tying `EN` to a rail would cost microamps continuously
- **WHEN** the driver is captured
- **THEN** `EN` connects to a SoC GPIO and to no pull-up

Requirement: Actuator off-board on a two-way connector

A coin linear resonant actuator SHALL connect through a **two-way connector**. It is off-board because the actuator is a mechanical selection that will change, and its resonant frequency and start current are open items. (KYR-403)

Scenario: Actuator is swapped during the study

- **GIVEN** open item O1 leaves the actuator part unselected
- **WHEN** a different coin LRA is fitted to J3
- **THEN** no board change is required, and the bank is re-evaluated against its measured start current

Requirement: Haptic capacitor bank fed through a series impedance

A **haptic capacitor bank** SHALL sit on the driver's supply node, fed from the cell through a ferrite bead or series resistance, so the actuator's start transient is drawn from the bank and not from the cell. The bank SHALL be sized from the actuator's start current and the intended pulse length, with the calculation stated in the specification, and SHALL be provided as **at least two parallel low-ESR capacitors**. (KYR-404, decision 5)

Scenario: Start transient does not brown out the radio

- **GIVEN** a 20 mAh cell at its 3 C limit delivers about 60 mA, and an LRA draws well over 100 mA at start
- **WHEN** the actuator starts while a BLE link is connected
- **THEN** the bank supplies the excess (97 mA of a 150 mA peak for 10 ms) and the cell supplies at most 53 mA, inside its 3 C limit
- **AND** `VDRV` droops 0.71 V, inside the 0.8 V budget, staying above the driver's 2.7 V floor

Scenario: Bank sizing is stated, not asserted

- **GIVEN** KYR-404 requires the calculation in the specification
- **WHEN** `docs/SPEC.md` §5.6 is read
- **THEN** it shows $\Delta V = 0.8$ V, $R_{HAP} \geq \Delta V/60$ mA = 13.3 Ω → 15 Ω, $C \geq 0.97$ mC/0.8 V = 1213 µF
- **AND** the fitted bank is 2×680 µF polymer, ESR ≤ 25 mΩ each

Scenario: A ferrite bead is proposed instead of a resistor

- **GIVEN** a ferrite bead is near 0 Ω at DC
- **WHEN** a bead is proposed as the series element
- **THEN** it is rejected for this board: the DC resistance is the entire mechanism that bounds the cell's current, and a bead would not bound it at all

Scenario: Pulses are spaced for bank recharge

- **GIVEN** $\tau = 15\ \Omega \times 1360\ \mu F = 20.4$ ms and 99 % recharge ≈ 102 ms
- **WHEN** a multi-pulse pattern is played
- **THEN** pulses are spaced ≥ 150 ms, and a three-pulse escalation occupies ≥ 450 ms

Scenario: The actuator is driven straight from the cell

- **GIVEN** direct drive browns out the radio and ages the cell
- **WHEN** a change removes the bank or the series element
- **THEN** the change is rejected: the bank is a hard requirement, not an optimisation

Requirement: At least three distinguishable haptic patterns

The haptic vocabulary SHALL support at least three distinguishable patterns: *something needs you*, *sent*, *dismissed*. The hardware obligation is bandwidth and rise time; the patterns are firmware. (KYR-405)

Scenario: Hardware does not limit the vocabulary

- **GIVEN** the driver tracks resonance and the bank holds the supply up
- **WHEN** three patterns differing in pulse count, length and spacing are played
- **THEN** each starts and stops within the actuator's rise time without supply-limited blurring

Scenario: Escalation is suppressed when not worn

- **GIVEN** KYR-206 gates escalation on wear detection
- **WHEN** the ring reads as not worn
- **THEN** no pattern is played regardless of the queued escalation

PART X

Capability: Bring-up and Instrumentation

Source: openspec/specs/instrumentation/spec.md

Source requirements: KYR-801 … KYR-805 (`brief.md` §8). See `docs/SPEC.md` §10, §5.7.

ADDED Requirements

Requirement: Serial wire debug on a 2x5 1.27 mm header with reset

The board SHALL carry serial wire debug on a **2×5 1.27 mm header, with the reset line included**. This is EV1 only; the ring has test pads. (KYR-801)

Scenario: Debugger can halt a running part

- **GIVEN** `SWDIO`, `SWDCLK` and `nRESET` are all present on the header
- **WHEN** a debug probe is attached
- **THEN** it can halt, flash and reset the SoC without additional wiring

Scenario: The ring build drops the header

- **GIVEN** the production ring has no room for a 2×5 header
- **WHEN** the ring is built
- **THEN** the same signals appear as test pads, and the header is EV1-only

Requirement: Current-measurement jumper in the cell's positive leg

The board SHALL carry a **current-measurement jumper in series with the cell's positive leg**, as a two-way header with a shorting link fitted for normal operation, so the average current of Q3 can be measured with an instrument. (KYR-802)

Scenario: Average current is measured on an instrument

- **GIVEN** Q3 asks whether the design holds 150 µA average on an instrument, not a spreadsheet
- **WHEN** the shorting link on J7 is replaced by a current meter
- **THEN** the entire board's supply current flows through the meter
- **AND** no path bypasses J7 between `VBAT_CELL` and `VBAT`

Scenario: Normal operation without an instrument

- **GIVEN** the board is used for anything other than the current measurement
- **WHEN** the shorting link is fitted
- **THEN** the board runs normally

Scenario: The jumper is deleted to save a part

- **GIVEN** it is the single most important part on the board for the purpose the board exists for
- **WHEN** a change proposes removing J7

- **THEN** the change is rejected: without it, Q3 has only a spreadsheet answer

Requirement: Minimum test point set

The board SHALL carry at least these test points: cell positive, the rectified node, the driver's supply node **ahead of and behind** the bank, the controller's VDD, the touch CHANGE line, the accelerometer interrupt line, and ground - with **at least two ground test points, physically separated**, so a scope probe can find a short return path. (KYR-803)

Scenario: The bank's effect is observable

- **GIVEN** test points on both `VBAT` (ahead of the bank) and `VDRV` (behind it)
- **WHEN** an LRA pulse is fired with a scope on both
- **THEN** the droop on each is measured separately, answering Q2 directly

Scenario: A probe finds a short return

- **GIVEN** two ground test points placed apart on the board
- **WHEN** a scope probe is attached near any signal test point
- **THEN** a ground point is close enough for a short return path, avoiding a long ground lead

Scenario: Interrupt timing is observable

- **GIVEN** test points on `TCH_CHANGE` and `ACC_INT`
- **WHEN** a gesture is made
- **THEN** the interrupt-to-wake latency is measurable for Q1

Scenario: No test point exists without a question

- **GIVEN** only Q1–Q4 justify instrumentation
- **WHEN** an additional test point is proposed
- **THEN** it is added only if it serves one of the four questions

Requirement: One charge-status LED with its resistor

The board SHALL carry exactly **one** charge-status LED with its series resistor. (KYR-804, decision 6)

Scenario: The only LED on the board

- **GIVEN** decision 6 forbids an indicator on the ring
- **WHEN** the schematic is reviewed
- **THEN** exactly one LED is present, it is the charge-status LED, and it is in the instrumentation block

Scenario: A status or power LED is proposed

- **GIVEN** an indicator on your hand is a notification other people can read
- **WHEN** any additional LED is proposed
- **THEN** it is rejected: the escalation channel is haptic and nothing else

Requirement: I2C bus pull-ups valued for the bus capacitance

The board SHALL carry I2C pull-ups valued for the bus's total capacitance at the intended speed. **One bus** serves the touch controller, the accelerometer and the haptic driver, and the three addresses SHALL be confirmed non-colliding and recorded in the pinout. (KYR-805)

Scenario: Pull-up value is derived from a rise-time budget

- **GIVEN** C_b ≈ 50 pF (ASSUMED A13) and fast-mode t_r(max) = 300 ns
- **WHEN** the bounds are computed
- **THEN** R_max = 300 ns / (0.8473 × 50 pF) = 7.08 kΩ and R_min = 2.6 V / 3 mA = 867 Ω
- **AND** 4.7 kΩ is fitted, giving a 199 ns rise time and 0.55 mA of sink current

Scenario: Addresses do not collide

- **GIVEN** three devices share one bus
- **WHEN** addresses are assigned
- **THEN** they are AT42QT1070 = 0x1B, KX022-1020 = 0x1E, DRV2605L = 0x5A, all distinct
- **AND** they are recorded in `docs/PINOUT.md`

Scenario: Pull-ups do not spend the standby budget

- **GIVEN** the bus idles high
- **WHEN** the current budget is itemised
- **THEN** the pull-up row is 0.1 µA, because current flows only during active-low bits

PART XI

Capability: Motion Interlock

Source: openspec/specs/motion-interlock/spec.md

Source requirements: KYR-301 … KYR-303 (`brief.md` §3). Budgets in `docs/SPEC.md` §4.2.

ADDED Requirements

Requirement: Three-axis accelerometer with wake-up engine

The board SHALL carry a three-axis accelerometer with an on-chip wake-up engine and a sample buffer, low-power current in single-digit microamps, on I2C (`Sensor_Motion:KX022-1020`). Its interrupt line SHALL go to the controller. (KYR-301)

Scenario: Accelerometer wakes the controller

- **GIVEN** the KX022-1020 wake-up engine is armed at 12.5 Hz ODR in low-power mode
- **WHEN** the hand is raised
- **THEN** the part asserts `ACC_INT` to a SoC GPIO
- **AND** the SoC reads the buffered samples over I2C rather than polling continuously

Scenario: Single-digit microamp budget row is honoured

- **GIVEN** KYR-301 requires low-power current in single-digit microamps
- **WHEN** the current budget is itemised
- **THEN** the accelerometer row is 8.7 μA (datasheet typ, wake-up engine, 12.5 Hz ODR)
- **AND** that row is below the 15 μA KYR-903 justification threshold

Scenario: Interface strapping is fixed in hardware

- **GIVEN** the KX022-1020 selects SPI unless told otherwise
- **WHEN** the part is captured
- **THEN** `CS` is tied to `VDD` to select I2C and `ADDR` is tied to `GND` to select 0x1E
- **AND** neither strap pin is driven from a GPIO

Requirement: Accelerometer only, no gyroscope or magnetometer

The board SHALL carry an accelerometer only. There SHALL be **no gyroscope and no magnetometer**: raise-and-settle is an accelerometer question and a gyroscope costs current for nothing. (KYR-302)

Scenario: An IMU is proposed

- **GIVEN** a six-axis IMU would answer the same raise-and-settle question
- **WHEN** a change proposes substituting one
- **THEN** the change is rejected on the current budget, because the gyroscope adds milliamp-class current against a 150 μA target

Requirement: No motion data leaves the ring

Accelerometer output SHALL be consumed **locally** as the confirm interlock. It SHALL NOT be logged, transmitted or aggregated, and no activity, sleep or step data SHALL be derived from it. (KYR-303, decision 4)

Scenario: Confirm is gated on the hand having meant it

- **GIVEN** the documented failure mode of gesture wearables is a false trigger while the hand is doing something else
- **WHEN** the strip reports a confirm gesture
- **THEN** the confirm is accepted only if the accelerometer reports the hand raised and settled

Scenario: An advertisement or characteristic exposes motion

- **GIVEN** the accelerometer is an interlock, not a sensor feature
- **WHEN** any BLE characteristic, log or advertisement payload is defined
- **THEN** none of them carries accelerometer data, raw or derived

Scenario: Activity tracking is requested as a feature

- **GIVEN** the hardware could physically produce step counts
- **WHEN** such a feature is proposed
- **THEN** it is refused: Kyra R1 is a control device, not a capture device, and this is the hardware expression of "your data stays with you"

PART XII

Capability: Pairing and Identity

Source: openspec/specs/pairing-identity/spec.md

Source requirements: KYR-701 … KYR-703 (`brief.md` §7), decision 10. See `docs/SPEC.md` §6.

ADDED Requirements

Requirement: NFC tag antenna on the dedicated pins, brought out on a connector

The board SHALL carry a near-field communication tag antenna on the controller's **dedicated NFC pins**, with the two tuning capacitors the vendor's reference requires, brought out on a two-way connector so the antenna is a mechanical part. This is out-of-band pairing: tap the ring to the host and pair with no PIN and no account. (KYR-701)

Scenario: Tap to pair

- **GIVEN** a host that supports NFC out-of-band pairing
- **WHEN** the ring is tapped to the host
- **THEN** pairing completes with no PIN, no account and no cloud

Scenario: NFC pins are left at their default function

- **GIVEN** P0.09 and P0.10 default to NFC under UICR `NFCPINS`
- **WHEN** GPIO is allocated
- **THEN** P0.09 and P0.10 are used as `NFC1`/`NFC2` and are excluded from the GPIO pool
- **AND** the two vendor-reference tuning capacitors are fitted across them

Scenario: The antenna is a mechanical part

- **GIVEN** the ring's NFC antenna geometry is a mechanical decision
- **WHEN** a different antenna is fitted to J8
- **THEN** no board change is required

Requirement: Gesture-confirmed pairing where NFC is unavailable

Where a host does not support near-field pairing, pairing SHALL be confirmed by a **deliberate gesture on the ring's own touch strip**. No extra hardware. (KYR-702, decision 10)

Scenario: Host without NFC

- **GIVEN** a host that cannot do out-of-band NFC pairing
- **WHEN** pairing is initiated from the host
- **THEN** the ring requires a deliberate confirm gesture on the strip before completing
- **AND** that gesture is subject to the same wear and motion interlocks as any other confirm

Scenario: No pairing hardware is added

- **GIVEN** the parts budget forbids unlisted circuitry
- **WHEN** a pairing button or display is proposed
- **THEN** it is rejected: the confirm surface the product is built on is the pairing surface

Requirement: No user-facing identifier in the advertisement

There SHALL be no user-facing identifier, serial-number readout, or advertisement payload carrying anything about the wearer. The advertisement SHALL carry a **rotating resolvable private address**. (KYR-703)

Scenario: Advertisement cannot be used to track the wearer

- **GIVEN** a passive observer logging BLE advertisements
- **WHEN** the ring advertises over time
- **THEN** the address is a rotating resolvable private address and does not correlate across rotations for an observer without the identity resolving key

Scenario: No serial number is readable

- **GIVEN** a connected but unbonded peer
- **WHEN** it enumerates characteristics
- **THEN** no serial number, device identifier or wearer attribute is exposed

Scenario: The escalation queue holds no content

- **GIVEN** the pending-escalation queue lives in internal flash (decision 7)
- **WHEN** its records are inspected
- **THEN** each holds an **opaque escalation identifier and a haptic pattern index, never message content**
- **AND** this is a product claim, recorded in `docs/SPEC.md`, not an implementation detail

PART XIII

Capability: Power Budget

Source: openspec/specs/power-budget/spec.md

Source requirements: KYR-901 … KYR-904 (`brief.md` §9). The budget itself is `docs/SPEC.md` §4.

ADDED Requirements

Requirement: 150 uA average target with a 177 uA ceiling

The design target SHALL be **150 μA average** and the ceiling SHALL be **177 μA**, over a duty cycle of **40 escalations and 40 gesture interactions per day**. 17 mAh usable from a 20 mAh cell over 96 hours is 177 μA; four days between charges is the bar the category has set. (KYR-901)

Scenario: Budget is below the target

- **GIVEN** the itemised table sums to 89.4 μA plus 20 % contingency
- **WHEN** the total is compared with the target
- **THEN** the budget total is 107.3 μA, leaving 42.7 μA of margin against 150 μA and 69.7 μA against 177 μA

Scenario: Endurance meets the four-day bar

- **GIVEN** 17 mAh usable and a 107.3 μA budget total
- **WHEN** endurance is computed
- **THEN** it is 158 h $\approx$ 6.6 days, comfortably beyond the 96 h bar
- **AND** at the 177 μA ceiling it is exactly 96 h, which is what makes 177 μA the ceiling

Scenario: A change pushes the total over the ceiling

- **GIVEN** 177 μA is a hard ceiling, not a target
- **WHEN** a proposed change raises the itemised total above 177 μA
- **THEN** the change is refused, or an existing row is reduced to pay for it

Scenario: The measured result disagrees with the budget

- **GIVEN** Q3 requires an instrument, not a spreadsheet
- **WHEN** the measured average through J7 exceeds the ceiling
- **THEN** the AT42QT1070 LP scan interval is the first tuning knob and the BLE connection interval is the second, both named in `docs/SPEC.md` §4.3

Requirement: Itemised current table, one row per device

The specification SHALL carry an **itemised current table**, one row per device, each row citing a datasheet figure and a stated operating mode, summed, with the margin against KYR-901 shown. **An unitemised total is not a budget.** (KYR-902)

Scenario: Every row names its mode and source

- **GIVEN** the table in `docs/SPEC.md` §4.2
- **WHEN** any row is inspected
- **THEN** it names the device, the operating mode, the current, and the figure's origin (datasheet typ, datasheet max, power profiler, derived, or allowance)

Scenario: Zero rows are stated, not omitted

- **GIVEN** several items legitimately contribute nothing
- **WHEN** the table is read
- **THEN** the charge LED, the `VRECT_SENSE` divider, the clamp and the absent battery-sense divider are each listed as zero with the reason, so a reader can tell a considered zero from an oversight

Scenario: A summary figure is offered without itemisation

- **GIVEN** KYR-902 forbids an unitemised total
- **WHEN** a change updates the budget with only a new total
- **THEN** it is rejected until the affected rows are updated

Requirement: Every part's standby current checked at selection

Every part's quiescent, standby and leakage current SHALL be checked against KYR-901 during part selection. **A part whose standby current alone spends a tenth of the budget must be justified in its rationale or replaced.** (KYR-903)

Scenario: A part exceeds a tenth of the target

- **GIVEN** a tenth of the 150 μA target is 15 μA
- **WHEN** a part's row exceeds 15 μA
- **THEN** its rationale column carries an explicit justification
- **AND** the two such parts, the AT42QT1070 at 40 μA and BLE link maintenance at 22 μA, are justified in `docs/SPEC.md` §4.3

Scenario: The touch controller's cost is justified

- **GIVEN** the AT42QT1070 spends 27 % of the target
- **WHEN** its justification is reviewed
- **THEN** it is the entire gesture surface and the reason the SoC can sleep; the alternatives (SoC-side scanning, or a second MCU as the open-ring reference uses) cost more current or a whole additional die

Scenario: A new part is proposed without a current figure

- **GIVEN** KYR-903 requires the check at selection time
- **WHEN** a part is proposed with no quiescent figure cited
- **THEN** it is not committed to the BOM until the figure is found and added to the table

Requirement: Haptic energy amortised into the budget

Haptic energy SHALL be amortised into the budget, stating the **per-pulse charge**, the **assumed pulses per day**, and the **resulting average**. (KYR-904)

Scenario: Escalation energy is amortised

- **GIVEN** 55 mA average supply current for a 3 $\times$ 60 ms escalation pattern
- **WHEN** the per-event charge is computed
- **THEN** it is 55 mA $\times$ 0.18 s = 9.9 mC = 2.75 μAh, and 40 per day gives **4.6 μA average**

Scenario: Acknowledgement energy is amortised

- **GIVEN** a 30 ms acknowledgement pulse at the same 55 mA
- **WHEN** the per-event charge is computed
- **THEN** it is 1.65 mC = 0.46 μAh, and 40 per day gives **0.8 μA average**
- **AND** the total haptic contribution is 5.4 μA, 3.6 % of the target

Scenario: The actuator turns out to draw more

- **GIVEN** open item O1 leaves the actuator's start current unknown (ASSUMED A5, A6)
- **WHEN** the real actuator is measured
- **THEN** the haptic rows and the bank sizing in `docs/SPEC.md` §5.6 are both recomputed

PART XIV

Capability: Thumb Interface

Source: openspec/specs/thumb-interface/spec.md

Source requirements: KYR-201 … KYR-206 (`brief.md` §2). Budgets in `docs/SPEC.md` §4.3, §5.7, §5.8.

ADDED Requirements

Requirement: Autonomous burst-mode capacitive touch controller

The board SHALL use a seven-channel burst-mode capacitive touch controller with an I2C interface and a CHANGE output (`Sensor_Touch:AT42QT1070-M`). It SHALL scan autonomously in low-power mode and interrupt the controller; **the controller SHALL NOT poll it**. (KYR-201)

Scenario: The SoC sleeps between gestures

- **GIVEN** the touch controller scans autonomously in low-power mode
- **WHEN** no thumb is present
- **THEN** `TCH_CHANGE` stays inactive and the SoC remains in System ON without waking
- **AND** the SoC's CPU row of the current budget stays at 80 wake events per day, not a continuous polling stream

Scenario: A gesture raises one interrupt

- **GIVEN** the thumb contacts the strip
- **WHEN** the controller detects a key change
- **THEN** it asserts `TCH_CHANGE` to a SoC GPIO, and the SoC reads the key state over I2C

Scenario: Touch on the SoC is proposed instead

- **GIVEN** the SoC has no charge-transfer peripheral, and GPIO or comparator methods cost a continuous stream of wake-ups
- **WHEN** a change proposes moving touch onto the SoC or adding a second MCU
- **THEN** the change is rejected: one autonomous controller with an interrupt is the whole power budget (decision 2)

Requirement: Fixed channel allocation

Channel allocation SHALL be fixed as: **three channels** as a linear strip along the ring's outer face for tap position and swipe direction, **one channel as the guard** encircling the strip, and **one channel as the wear-detect electrode** on the inner face. The remaining two channels SHALL be spare and terminated per the datasheet. (KYR-202)

Scenario: Seven channels are accounted for

- **GIVEN** the AT42QT1070 has seven keys
- **WHEN** the channel map is written into `docs/PINOUT.md`
- **THEN** three are `E_STRIP1`..`E_STRIP3`, one is `E_GUARD`, one is `E_WEAR`, and two are spare and terminated as the datasheet requires

Scenario: Three-gesture grammar is supported

- **GIVEN** the product needs reply, dismiss and confirm
- **WHEN** the three strip channels are read in sequence
- **THEN** tap position and swipe direction are both resolvable from the three channels

Requirement: Electrodes are off-board on a flat-flex connector

The electrodes SHALL NOT be on this board. They SHALL leave on a **six-way flat-flex connector** (three strip, one guard, one wear, one ground), so electrode geometry, pitch and guard width can be changed without a board spin. (KYR-203)

Scenario: Electrode geometry is changed during the study

- **GIVEN** electrode geometry is the experiment (open item O5)
- **WHEN** a new electrode flex with a different strip pitch is fitted to J4
- **THEN** no board change is required

Scenario: A fixed copper electrode pattern is proposed

- **GIVEN** a fixed copper pattern would defeat the experiment
- **WHEN** a change proposes electrodes on the PCB
- **THEN** the change is rejected

Scenario: The flex carries its own ground

- **GIVEN** high-impedance charge-transfer lines need a return
- **WHEN** J4 is wired
- **THEN** one of the six ways is `GND`

Requirement: Series resistors on every electrode line

The board SHALL fit a series resistor on **every** electrode line, placed close to the controller, for electrostatic-discharge and radiated-emissions control. The value SHALL be recorded with its reason. (KYR-204)

Scenario: Value and reason are recorded

- **GIVEN** KYR-204 requires the value to be a recorded design decision
- **WHEN** `docs/SPEC.md` §5.8 is read
- **THEN** the value is 1 kΩ 0402, with the reason: ESD/EMI limiting on lines leaving the board on a flex tail, at the low end of the QTouch 1 kΩ–10 kΩ guidance because the leads are long and extra series resistance costs sensitivity

Scenario: Acquisition is not degraded

- **GIVEN** electrode capacitance of 5–20 pF and a 1 kΩ series resistor
- **WHEN** the RC time constant is compared with the charge-transfer burst timing
- **THEN** $RC \leq 20$ ns is negligible against microsecond-scale bursts

Scenario: All six lines are protected

- **GIVEN** six lines leave on the flex (five electrodes plus ground)
- **WHEN** the series resistors are placed

- **THEN** each of the five electrode lines carries one, hard against the controller

Requirement: Adjacent key suppression and guard channel enabled

Adjacent key suppression and the guard channel SHALL **both** be enabled. The specification SHALL record that the wet-hand result is a **measurement to be taken, not a claim**. (KYR-205)

Scenario: Guard is mandatory, not optional

- **GIVEN** self capacitance was chosen over mutual capacitance for size, cost and availability
- **WHEN** the channel map is fixed
- **THEN** one channel is permanently allocated to the guard and cannot be reassigned

Scenario: No wet-hand performance is claimed

- **GIVEN** mutual capacitance rejects water films and body loading better
- **WHEN** the specification describes wet-hand behaviour
- **THEN** it makes no claim, and states that Q1 is the test of whether self capacitance was the right call

Scenario: Q1 fails

- **GIVEN** the guard channel does not rescue wet-hand performance
- **WHEN** the Q1 result is recorded
- **THEN** the production ring moves to a mutual-capacitance controller and nothing else in the architecture changes

Requirement: Wear detection gates product behaviour

When the ring reads as **not worn**, it SHALL NOT raise a haptic escalation and SHALL NOT accept a confirm. The hardware obligation is the electrode and the channel; the rule is firmware and belongs in the specification. (KYR-206)

Scenario: Ring on the desk

- **GIVEN** the wear-detect channel reads not worn
- **WHEN** an escalation arrives over BLE
- **THEN** no haptic pulse is produced, and the escalation stays queued

Scenario: Confirm attempted while not worn

- **GIVEN** the wear-detect channel reads not worn
- **WHEN** the strip reports a confirm gesture
- **THEN** the confirm is rejected

Scenario: Hardware provides the channel

- **GIVEN** the rule is firmware
- **WHEN** the board is captured
- **THEN** `E_WEAR` exists as a dedicated channel on the inner face, so firmware can enforce it

PART XV

Capability: Wireless Receive Front End

Source: openspec/specs/wireless-receive/spec.md

Source requirements: KYR-601 … KYR-606 (`brief.md` §6). Budgets in `docs/SPEC.md` §5.3–§5.5, §5.9.

ADDED Requirements

Requirement: Receive coil on a two-way connector

The receive coil SHALL connect through a **two-way connector**. Coil geometry, inductance and quality factor are open items and will change during the link study. (KYR-601)

Scenario: The coil is changed during the link study

- **GIVEN** open item O3 leaves coil geometry, L, Q and coupling unknown
- **WHEN** a different coil is fitted to J6
- **THEN** no board change is required, and only the resonant capacitor is re-derived

Scenario: Charging is contactless by design

- **GIVEN** the ring is sealed and hand-washed
- **WHEN** the charging interface is chosen
- **THEN** it is inductive, because an exposed contact is the seal that fails first

Requirement: Series resonant capacitor with a trim position

The series resonant capacitor SHALL be sized with the coil for the link frequency, with a **second footprint in parallel** so the resonance can be trimmed on the bench. (KYR-602)

Scenario: Resonance is computed from the assumed coil

- **GIVEN** L = 1.0 μH (ASSUMED A11) and f = 6.78 MHz (ASSUMED A10)
- **WHEN** C_RES = $1/((2\pi f)^2 L)$ is evaluated
- **THEN** C_RES = 551 pF, fitted as **560 pF C0G 0402 50 V**

Scenario: Resonance is trimmed without a board spin

- **GIVEN** the coil's true inductance will differ from the assumption
- **WHEN** the link is tuned on the bench
- **THEN** a second parallel 0402 position, unpopulated at build, accepts the trim capacitor

Requirement: Schottky full-wave rectifier selected for low parasitic capacitance

The rectifier SHALL be full-wave, built from Schottky diodes selected for **low parasitic capacitance at the link frequency, not for lowest forward voltage**. Dual packages are preferred for area (`Diode:BAT54S` class). (KYR-603, decision 9)

Scenario: Selection criterion is capacitance, not V_F

- **GIVEN** Q4 asks whether the rectifier's diode capacitance is the dominant loss
- **WHEN** two candidate Schottkys are compared
- **THEN** the one with lower junction capacitance is chosen even if its forward voltage is higher
- **AND** the chosen part's C_j at the link frequency is recorded in the BOM rationale

Scenario: Area is conserved with dual packages

- **GIVEN** a full-wave bridge needs four diodes and the board is 20×20 mm
- **WHEN** the bridge is captured
- **THEN** two dual-diode packages are used rather than four singles

Scenario: An integrated LF wireless-power receiver is proposed

- **GIVEN** the ring's coil is a megahertz-class part
- **WHEN** a low-frequency wireless-power receiver IC is proposed instead of the discrete front end
- **THEN** it is rejected: it would be thrown away at the flex spin (decision 9)

Requirement: Clamp and bulk capacitor on the rectified node

A clamp SHALL sit on the rectified node so an over-coupled or unloaded link cannot push the charger's input above its absolute maximum: a Zener or TVS diode plus a bulk capacitor sized to hold the charger's input through the ripple. (KYR-604)

Scenario: Unloaded link cannot destroy the charger

- **GIVEN** the MCP73831's absolute-maximum input is 7 V
- **WHEN** the link is over-coupled or unloaded and `VRECT` rises
- **THEN** the clamp holds `VRECT` at 5.1 V ± 5 %, at most 5.36 V, below the 6.0 V design ceiling and well below 7 V

Scenario: The clamp window is derived, not chosen arbitrarily

- **GIVEN** the charger needs headroom above a 4.2 V full cell
- **WHEN** the window is derived
- **THEN** the lower bound is 4.2 + 0.3 = 4.5 V and the upper bound is $7 - 1 = 6.0$ V, and 5.1 V sits inside it at both tolerance extremes

Scenario: Bulk holds the input through the ripple

- **GIVEN** C_RECT = 10 μF and 15 mA of charge current
- **WHEN** ripple and hold-up are computed
- **THEN** ripple at 6.78 MHz is ≈ 0.11 mV and hold-up for a 0.9 V droop is 0.6 ms
- **AND** a longer interruption merely pauses charging, which is acceptable

Scenario: Clamp power rating is confirmed against the dock

- **GIVEN** the transmitter's delivered power is out of scope (KYR-606)
- **WHEN** the 500 mW clamp rating (ASSUMED A12) is reviewed
- **THEN** it is confirmed against the dock design before the link study runs

Requirement: Rectified-voltage sense into a controller analog input

The rectified voltage SHALL be sensed into a controller analog input through a divider, so the link's delivered voltage can be logged during the link study. **This is the one divider the board carries and it exists for Q4.** (KYR-605)

Scenario: Delivered voltage is logged

- **GIVEN** R_top = 1 MΩ and R_bot = 470 kΩ
- **WHEN** `VRECT` is at its 5.4 V worst case
- **THEN** the ADC sees 1.73 V, inside the 3.0 V `VDD` reference range

Scenario: The divider costs nothing off the dock

- **GIVEN** the divider sits on `VRECT`, not on `VBAT`
- **WHEN** the ring is off the dock and `VRECT` is 0 V
- **THEN** the divider draws zero from the cell, which is why it is placed on the rectified node rather than after the charger

Scenario: ADC acquisition time matches the source impedance

- **GIVEN** the divider's source impedance is 1 M || 470 k = 320 kΩ
- **WHEN** the SAADC is configured
- **THEN** acquisition time is at least 20 μs, not the 10 μs default

Scenario: A second divider is proposed for battery sense

- **GIVEN** decision 8 deletes the battery-sense divider
- **WHEN** a change proposes a divider on `VBAT`
- **THEN** it is rejected: the SoC measures VDDH through the SAADC internal divider input, which deletes a divider, a switch to stop it leaking, and the routing for both

Requirement: Transmitter and dock are out of scope

The transmitter, the dock and its resonant drive SHALL be a **separate board and out of scope**. This board is the **receiver only**. (KYR-606)

Scenario: Dock circuitry is proposed for this board

- **GIVEN** the parts budget forbids circuitry not listed as a board requirement
- **WHEN** transmitter or resonant-drive circuitry is proposed
- **THEN** it is rejected as out of scope

Scenario: ISM regulatory obligation is placed correctly

- **GIVEN** the induction link runs in an ISM band
- **WHEN** compliance is assessed
- **THEN** the obligation falls mainly on the transmitter, which is out of scope here

PART XVI

Proposal: architecture-subsystem-decomposition

Source: openspec/changes/architecture-subsystem-decomposition/proposal.md

Marker: AUTO (autonomous mode; auto-approved, reviewable after the fact)

Why

Stage 1 produced a requirements spec organised by requirement id (KYR-xxx) and by calculation. Nothing yet states the board as a set of subsystems with owned boundaries, owned budget shares and owned interface nets. Capture cannot start from a calculation list: it needs to know which block owns VDRV, which block owns the 40 uA that dominates the budget, and what each block is allowed to spend before it steals from another. docs/SUBSYSTEMS.md is that decomposition. It introduces no new parts, no new nets and no new numbers - every value is traced back to a SPEC.md section or a constraints.json key - but it partitions the 89.4 uA itemised sub-total and the ~92-98 symbol estimate across nine subsystems so that later stages can tell whether a change is local or is spending someone else's margin.

What Changes

- **NEW** `docs/SUBSYSTEMS.md`: prose block diagram (power flow and signal flow described in words, not ASCII), then one section per subsystem: 1 cell + protection + rails, 2 charging, 3 wireless receive front end, 4 controller and radio, 5 connectivity (BLE antenna + NFC pairing), 6 thumb interface, 7 motion interlock, 8 haptic escalation, 9 instrumentation.
- Each section carries: purpose, the parts it owns (confirmed lib_ids only, from SPEC §3.2), the nets it owns and the nets it consumes, its **current allocation** in uA, its **symbol allocation**, its key sized values, and the reasoning for each.
- Cross-subsystem tables: (a) current rollup by subsystem summing to exactly 89.4 uA, the SPEC §4.2 itemised sub-total; (b) symbol rollup by subsystem; (c) an interface contract table listing every net that crosses a subsystem boundary with its producer and consumers; (d) the four cross-domain hazards (3.0 V bus into a VDRV-powered DRV2605L, cell to VDDH never VDD, high-Z electrode lines vs the DC-DC and rectifier, 320 kOhm ADC source impedance).
- A deliberate-absences section restating each forbidden block/part as an architectural choice with its decision number, so a reviewer cannot read a missing pullup or a missing regulator as an oversight.
- `docs/SPEC.md` **§3.7 (edit, arithmetic only)**: the per-block symbol table's rows sum to 101 at the top of their '~' ranges while the stated total is 92-98. Add one line recording the worst-case sum and that ceiling headroom is therefore 4 symbols, not 13. No block estimate is changed.
- `docs/CHANGELOG.md`: one entry for this run.

PART XVII

Tasks

Source: openspec/changes/architecture-subsystem-decomposition/tasks.md

- ☐ Re-read docs/SPEC.md §3.7 and §4.2 exactly as written before allocating, so no figure is paraphrased from memory
- ☐ Write docs/SUBSYSTEMS.md with the nine subsystem sections and the four cross-subsystem tables
- ☐ Verify the per-subsystem current allocations sum to 89.4 uA exactly against SPEC §4.2 rows 1-13
- ☐ Verify the per-subsystem symbol allocations reproduce SPEC §3.7 block by block
- ☐ Verify every net named in the interface contract table appears in the SPEC §3.4 canonical net list, with no additions
- ☐ Edit docs/SPEC.md §3.7 to record the worst-case symbol sum (101) and the true 4-symbol headroom
- ☐ Append the docs/CHANGELOG.md entry
- ☐ record_decision for the subsystem partition, the budget-ownership rule, and the symbol-headroom finding
- ☐ record_constraint for the per-subsystem budget shares and the corrected symbol headroom
- ☐ Run check_drift and reconcile anything it reports

PART XVIII

Proposal: part-selection-bom-ev1

Source: openspec/changes/part-selection-bom-ev1/proposal.md

Marker: AUTO (autonomous mode; auto-approved, reviewable after the fact)

Why

Stage 3 must turn the architecture into a per-refdes bill of materials that stage 4 can actually capture: every active part drawn from a symbol confirmed installed on this machine, every MPN flagged UNVERIFIED with a datasheet-checkable justification, and every part's quiescent/leakage current checked against the 150 uA target and 177 uA ceiling. Three SPEC values cannot be realised as written and are resolved here as recorded deviations rather than refusals: (1) the 1360 uF polymer haptic bank leaks 40-400 uA at its datasheet limit and cannot be bought at single-digit uA, (2) the installed nRF52833 symbol exposes DEC4/DCC but no DCCH, so REG0 must run as an LDO and the REG0 DC-DC inductor path is not capturable, (3) MCP73831-2 STAT is push-pull referenced to VRECT (5.1 V nominal, 5.4 V clamped max) and cannot be wired straight to a 3.0 V GPIO.

What Changes

- **NEW** `docs/BOM.md` - 91 rows, one per refdes, fixed table `| Refdes | Value | Footprint | MPN | Rationale |`. Value column holds only the component value; all prose in Rationale. Every MPN prefixed `UNVERIFIED:`.
- Every active part confirmed by `search_symbols + symbol_pins` on this machine: U1 `MCU_Nordic:nRF52833_QDxx` (41 pins), U2 `Sensor_Touch:AT42QT1070-M` (21), U3 `Sensor_Motion:KX022-1020` (11), U4 `Driver:DRV2605LDGS` (10), U5 `Battery_Management:MCP73831-2-OT` (5), U6 `Battery_Management:AP9101CK6` (6), Q1 `Transistor_FET:Q_Dual_NMOS_S1G1D2S2G2D1` (6 pins, 2 units), D2/D3 `Diode:BAT54S` (3), D4 `Device:D_Zener`, ANT1 `Device:Antenna_Chip`, J1 `Connector_Generic:Conn_02x05_Odd_Even`, J4 `Connector_Generic:Conn_01x06`, J3/J5/J6/J7/J8 `Connector_Generic:Conn_01x02`, TP1-9 `Connector:TestPoint`, H1/H2 `Mechanical:MountingHole`, Y1 `Device:Crystal_GND24`, Y2 `Device:Crystal`.
- **Deviation 1 - haptic bank.** 2 x 680 uF polymer replaced by C32-C35, 4 x 220 uF 6.3 V X5R 1210 MLCC (nominal 880 uF, ~308 uF effective after 65 % DC-bias derating at 3.7 V). Supports ~78 mA peak for 10 ms against the ASSUMED 150 mA (A5); firmware overdrive limiting required until O1 closes. Leakage budgeted at 2.0 uA (typical) with the datasheet IR limit noted as far worse and a J7 measurement obligation.
- **Deviation 2 - REG0 as LDO.** No DCCH pin on the installed symbol, so no REG0 buck inductor; REG1 buck retained (L1 10 uH on DCC-DEC4). Costs ~+3.6 uA (~4.6 % of the 75.5 uA that passes through REG0).
- **Deviation 3 - CHG_STAT level shift.** New R5/R6 100k/100k divider from STAT to GND, tap to GPIO: 2.55 V at nominal VRECT, 2.70 V at clamp max, and the bottom resistor defines the high-Z state as low. Draws 27 uA from the **dock**, zero from the cell.
- **Budget impact recorded, not hidden:** itemised sub-total 89.4 -> 95.0 uA, +20 % contingency -> **114.0 uA**. Still inside the 150 uA target (36 uA margin) and the 177 uA ceiling (63 uA), but **over the derived** `power.budget_total_uA` **= 107.3 uA bookkeeping figure** - logged as an open item for the human.
- `docs/SPEC.md`: §4.2 part-selection delta paragraph, §5.6 fitted-bank note, §12 new ASSUMED A23-A25, §13 new open items O9-O11.
- `docs/SUBSYSTEMS.md`: §3.2 (STAT level shift), §3.4 (REG0 LDO), §3.8 (fitted bank) notes.

- `docs/DECISIONS.md`: four entries, three flagged OPEN ITEM FOR HUMAN.
- `docs/CHANGELOG.md`: run entry.

PART XIX

Tasks

Source: openspec/changes/part-selection-bom-ev1/tasks.md

- ☐ Confirm every active symbol with search_symbols + symbol_pins (done for all ICs, FET, diodes, connectors, crystals, antenna, test point, mounting hole)
- ☐ Write docs/BOM.md, 91 rows, one refdes per row, no ranges, Value column = value only
- ☐ Check quiescent/leakage of every part against the S0-S9 allocations and restate the revised total
- ☐ Annotate SPEC.md §4.2, §5.6, §12, §13 with the three deviations
- ☐ Annotate SUBSYSTEMS.md §3.2, §3.4, §3.8
- ☐ Append DECISIONS.md entries, three flagged OPEN ITEM FOR HUMAN
- ☐ Append CHANGELOG.md entry
- ☐ Run check_drift and finish

PART XX

Proposal: seed-kyra-r1-ev1-requirements

Source: openspec/changes/seed-kyra-r1-ev1-requirements/proposal.md

Marker: AUTO (autonomous mode; auto-approved, reviewable after the fact)

Why

Stage 1 of the create pipeline for Kyra R1 EV1. The repo holds only brief.md: there is no docs/SPEC.md, no capability specs and no recorded constraints, so no later stage (part selection, capture, layout) has a budget to check itself against. The brief states hard numbers (150 uA average / 177 uA ceiling, 20 mAh cell, 15 mA charge, <=105 placed symbols, 20x20 mm, 0-45 C) and leaves several values open (actuator, coil, link frequency, electrode geometry). Those must be written down once, as budgets with owners, before anything is drawn, and every open value must be closed with a flagged default so stage 2 has numbers to capture.

What Changes

- Add `docs/SPEC.md`: device definition, EV1's four validation questions, scope and out-of-scope, block architecture with confirmed lib_ids, canonical net names, the full constraint and budget table, the itemised KYR-902 current budget (row per device, mode + cited figure, summed, contingency, margin against KYR-901), and the sizing calculations the brief demands: MCP73831 R_PROG for 15 mA, charger worst-case dissipation, haptic capacitor bank, I2C pull-ups, electrode series resistors, VRECT divider and clamp.
- Record every stated budget as a constraint: 150 uA target, 177 uA ceiling, 20 mAh cell / 17 mAh usable / 96 h, 15 mA charge (0.75 C), 60 mA (3 C) cell limit, <=105 placed symbols, 20x20 mm 2-layer, 0-45 C operating / -20-+60 C storage, 0402 minimum passive, VDDH 1.8-5.5 V, MCP73831 input abs-max 7 V (clamp <= 6.0 V), DRV2605L minimum supply, forbidden capture hardware.
- Record the closed decisions from the brief and the values this stage closes (VDD via REG0, 4.7 k I2C pull-ups, 1 k electrode series R, 10 ohm haptic series element, 2 x 470 uF bank, 5.1 V clamp, 1 M / 470 k VRECT divider, 66.5 k R_PROG, no on-board reset button).
- Seed `openspec/specs/` with nine capability specs (controller-radio, thumb-interface, motion-interlock, haptic-escalation, cell-charging, wireless-receive, pairing-identity, instrumentation, power-budget) carrying KYR-xxx requirement text as SHALL statements with Given/When/Then scenarios.
- Flag every value the brief did not state as ASSUMED and list the brief's open items verbatim, so stage 2 cannot silently adopt an assumption as fact.
- No schematic or board files exist or are touched in this stage; ERC/DRC/legibility are not applicable to a requirements seed.

PART XXI

Tasks

Source: openspec/changes/seed-kyra-r1-ev1-requirements/tasks.md

- ✓ Confirm every brief-named part resolves to an installed symbol before naming it in the spec
- ☐ Write docs/SPEC.md: device, four validation questions, scope, architecture + lib_ids, net names
- ☐ Write the constraint/budget table (parts count, mechanical, thermal, environment, electrical limits)
- ☐ Write the itemised current budget (KYR-902): row per device, mode, figure, source; sum; contingency; margin vs 150 uA and 177 uA; resulting runtime
- ☐ Write the sizing calculations: R_PROG = 1000V/I_REG; charger dissipation at the clamped input; haptic bank from start current and pulse length (KYR-404/904); I2C pull-up from bus capacitance; electrode series R; VRECT divider and clamp
- ☐ Write the privacy/product claims, compliance and environment sections
- ☐ List ASSUMED defaults and open items in one table each, with the requirement each blocks
- ☐ Seed openspec/specs/<capability>/spec.md for all nine capabilities with Given/When/Then scenarios
- ☐ record_constraint for every budget stated in docs/SPEC.md
- ☐ record_decision for each closed decision and each value this stage picks
- ☐ Run check_drift and finish

PART XXII

Attempt 01 - FAIL (operator stop)

Source: /home/animesh/copperhead/kyra/run-logs/2026-09-02T02-32-40/attempt-01/REPORT.md

Metadata: ./metadata.json Log: ./create.log Evidence: ./evidence/

What happened

Stage 1 (spec-seed), stage-attempt 1, turn 2 of 40, about 5m20s of wall time. The operator asked for the run to be stopped so that new client evidence could be reviewed. SIGINT was sent to the copperhead process only (PID 79653), not to the harness wrapper, and the wrapper then ran its evidence copy and wrote metadata normally. Exit 130. No stage completed and no document was written.

Failure mechanism

Operator termination. It is not one of the pipeline's failure classes: no timeout, no contract gap, no tool defect, no rollback, no resource exhaustion, no provider error, no budget or context event. Every reliability counter in metadata.json is zero.

Evidence

- `create.log`: `=== run end 2026-09-02T02:38:02+05:30 . exit=130 ===` directly after `still working - 4m30s elapsed (no output yet)` on turn 2.
- `evidence/2026-09-01T21-02-41-858Z/transcript.jsonl`: 1 run-start, 2 assistant, 4 tool events. The last tool calls are the seed searches (`search .`, `search openspec/**`, `read_file openspec/project.md` returning ENOENT, which is normal on a fresh workspace). No event type matches fail, refused, timeout, limit or restore.
- `evidence/git-status.txt`: `.copperhead/config.json` modified by init (expanded to its full form; `stageMaxTurns.part-selection=80` preserved) and `.copperhead/runs/` untracked. `evidence/git-stash.txt` is empty. Nothing was lost because nothing had been written.

Root cause

An engagement decision, not a defect. The evidence survived because the signal targeted the child process: `bin/run-attempt.sh` has no trap, so the same signal to the wrapper would have ended the script before the evidence copy (R21).

New or recurrence

No defect. One harness improvement filed: R21, a graceful stop and a stop-after-stage option in `run-attempt.sh`.

Action taken

None on copperhead. The workspace was left exactly as the run left it.

Validated

Not applicable.

Next attempt

Attempt-02, same brief and same config, variable "resume after operator stop". The brief is unchanged, so it lands in this session.

PART XXIII

Attempt 02 - FAIL (operator stop at the stage-4 boundary; stages 1 to 3 committed)

Source: /home/animesh/copperhead/kyra/run-logs/2026-09-02T02-32-40/attempt-02/REPORT.md

Metadata: ./metadata.json Log: ./create.log Evidence: ./evidence/

What happened

Stages 1 to 3 committed: spec-seed `786b723` (25m19s, 120.1k out), architecture `370678f` (11m01s, 49.9k out), part-selection `c19ab02` on its **second** stage-attempt (turn 38 of 80, 43m28s, 148.6k out). The first stage-attempt of part-selection ran 2h42m, 70 of 80 turns and 449.2k output tokens and ended `refused`. Stage 4 then began, scaffolded the empty KiCad project, and was stopped by the operator at its first turn: SIGINT to the copperhead child (PID 86933), wrapper left alive to copy evidence. Exit 130. The engagement's scope is stage 3, so this is the intended end of the run, not a failure of it.

Failure mechanism

Operator termination at the stage-4 banner. Inside stage 3, one stage-attempt was spent on an honest refusal against a budget the pipeline had itself derived (below).

Evidence

- `create.log`: `committed 786b723e54 (11 file(s)); committed 370678f926 (4 file(s)); refused . ERC not run . 2h42m . 70 in / 449.2k out; stage part-selection: diagnosis -> retry - The stated blockers are documentable design trade-offs, not missing inputs or tooling failures - the cited symbols all resolve on this machine and stage 3 can select parts while recording the open architecture questions instead of refusing.; committed c19ab021c9 (5 file(s)); === run end 2026-09-02T06:55:58+05:30 . exit=130 ===`.
- Transcript: 195 tool, 115 assistant, 7 `turn-timeout` (600 s watchdog: six in stage-3 attempt 1, one in attempt 2, every one recovered on the turn's second try), 1 `run-refused` at 00:41:22Z: *"Refused to commit docs/BOM.md: the specified haptic bank violates power.budget_total_uA (107.3 uA max), the S8 allocation (6.4 uA) and power.average_ceiling_uA (177 uA). PRIMARY BLOCKER - haptic bank leakage ..."*
- `metadata.json`: stages completed 3, stopped in schematic, stage_retries 1, watchdog_timeouts 7, provider_errors 0, rollbacks 0.
- Git: three stage commits. After the stop the tree holds stage 4's own scaffold, uncommitted (`*.kicad_sch`, `*.kicad_pcb`, `*.kicad_pro` untracked; `.copperhead/config.json` wired to them; `.copperhead/constraints.json` modified). No stash. Nothing from stage 3 is uncommitted.
- `docs/BOM.md` at `c19ab02`: 90 refdes against a ceiling of 105: 78 parts, 9 test points, 2 mounting holes, 1 DNP position. **All 78 part rows carry `UNVERIFIED: <MPN>` in the MPN column.** The 12 no-part rows carry a dash placeholder. Itemised idle draw 96.9 uA; 116.3 uA with 20 % contingency; predicted endurance 146 h.

Root cause

Two things worth naming; neither is a crash.

1. **Stage-3 attempt 1 refused on a self-derived budget.** Stage 1 had written `power.budget_total_uA` = 107.3 uA into the constraints as the itemised sum of its own allocations. The part-selection agent found that the SPEC's 2 x 680 uF polymer haptic bank leaks on the order of microamps, which breaks the S8 allocation and that derived total, and it refused to commit rather than record a deviation. The retry supervisor's diagnosis was right and specific. Attempt 2 replaced the bank with 4 x 220 uF X6S MLCC (about 308 uF effective), wrote it up as Deviation 1 in §4.1, and reported the revised total honestly in §4.4: within the 150 uA target and the 177 uA ceiling, 9 uA over the 107.3 uA derived figure. The refusal cost 2h42m and 449k output tokens for a finding that attempt 2 documented in a paragraph. Filed as R22.
2. **The I29 gate passed by accident.** The completion contract wants one BOM row whose MPN cell does not start with `UNVERIFIED`. Not one of the 78 part rows satisfies it. The twelve rows for test points, mounting holes and the DNP position, which carry a dash in the MPN column, do. A formatting choice on copper pads decided whether the stage passed. This is the third campaign to hit I29 and the first to pass it, and the pass proves the point: the gate is not measuring what it is meant to.

The seven watchdog timeouts are the known slow-turn pattern of stage 3 (symbol probing across 222 libraries and long BOM writes); dr-water's stage 3 recovered four the same way. Not new, and every one recovered.

New or recurrence

- **I27, not exercised here.** With `stageMaxTurns.part-selection=80`, stage 3 used 35 turns on the refused stage-attempt and 38 on the committed one (turn markers in create.log; the per-stage summary line's leading number is the I28 input counter, not a turn count, and an earlier revision of this report misread it as 70). Both sit under the default cap of 40, so the raised cap was not needed on the ring. The glasses' stage 3 used 46 and did need it.
- **I29 recurrence**, third campaign, with the new observation above.
- **R22 NEW.** A refusal against a budget the pipeline derived should be a documented deviation, and the supervisor's guidance should reach the agent before the refusal, not after a 2h42m stage-attempt.

Action taken

None on copperhead. Registers updated: I27, I29, R22, CURRENT-STATE.

Validated

Not applicable; no fix was made.

Next attempt

None for this brief within the engagement's scope: stage 3 is committed. If stage 4 is ever run, resume is automatic from `c19ab02`, and the uncommitted scaffold in the workspace is stage 4's own. On the design side, the bank now fitted supports (per the BOM's own rationale) about 78 mA for 10 ms within the droop budget, against the brief's assumption of about 100 mA for about 80 ms; that tension is recorded in the engagement's registers (OI-24) and is exactly what the ring EV1's question 2 measures.